NOVEL CURRENT-FED BOUNDARY-MODE PARALLEL-RESONANT PUSH-PULL CONVERTER

A Thesis

presented to

the Faculty of California Polytechnic State University,

San Luis Obispo

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

by

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June 2009

COMMITTEE MEMBERSHIP

TITLE: NOVEL CURRENT-FED BOUNDARY-MODE PARALLEL-RESONANT PUSH-PULL CONVERTER

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Abstract:

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Jonathan Paolucci

The inherent difficulty in designing high voltage power supplies is often compounded by demands of high reliability, high performance, and safe functionality. A proposed high step-up ratio DC-DC converter meets the exacting requirements of applications such as uninterruptible power systems, radar, and pulsed power systems. The proposed DC-DC converter topology combines a multi-phase buck input stage with a novel self-tracking zero-voltage-switching (ZVS) resonant output stage. Traditionally, the inclusion of multiple power processing stages within a power supply topology severely degrades the overall converter efficiency. Due to the inherent high efficiency per stage, however, this effect is minimized. The self-tracking switching scheme ensures that ZVS occurs across the full range of load variation. Furthermore, the switching scheme allows significantly increased flexibility in component tolerances compared to traditional resonant converter designs. The converter also demonstrates indefinite short-circuit protection and true ZVS during transient processes. Computer simulation and hardware analysis verify the efficacy of the topology as a rugged and efficient converter.

Acknowledgements

To Dr. Taufik – Thank you so much for your guidance and support over the years. I have you to thank for encouraging me to pursue post-graduate studies. As my thesis topic consists of 100% power electronics, you unknowingly laid the theoretical foundation onto which this topic has been built.

To Scott McClucky – Without a doubt, the success of this project would not have been possible without your help. Any accomplishments derived from this project are as much yours as they are mine. Thank you for truly being an inspiration and we all look forward to your future successes.

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Chapter 1: Introduction

1.1. Introduction to Power Electronics

The field of power electronics encompasses the control and conversion of electrical power by means of solid-state electronics. While power may range from milliwatts to megawatts, the building blocks of power electronic systems remains surprisingly unchanged. Solid-state switches control the flow of electrical energy from input to output through a variety of switching schemes. Integrated circuits and discrete components operate in conjunction with the power switches, providing the necessary signal conditioning, gate drive, and analog operations intrinsic to implementing power systems. In more complicated systems, microprocessors and signal processing integrated circuits coordinate and network circuit operations. The fusion of digital systems with high power electronics yields dynamic and intelligent systems that transparently adapt switching characteristics to meet demanding requirements.

As tomorrow's technological needs necessitate increased efficiency and power density within electrical systems, power electronics continues to expand into tangential engineering fields. Power electronics engineering involves the study and implementation of analog and digital circuits, electronic devices, control and power systems, magnetics, electric machines, and complex mathematical simulation tools. The combined advancements from each of these fields allow engineers to design systems with higher efficiency, increased power density, ruggedness of operation, and minimal electrical noise.

Power electronic systems are often classified in one of four categories:

1. DC-DC Converters: The magnitude of DC voltages is changed from input to output.
2. AC-DC Rectifiers: An alternating voltage is converted to a DC voltage.
3. DC-AC Inverters: A DC voltage is converted to a time-varying signal with a specified magnitude and frequency.
4. AC-AC Cycloconverters: An AC voltage is converted to an AC voltage with different magnitude and/or frequency.

The DC-DC converters are further classified into non-isolated and isolated topologies. The non-isolated topologies are most commonly used for on-board power supplies wherein isolation is not required. Examples of such topologies are buck, boost, and buck-boost converters. The isolated topologies, as the name implies, offer the provision of isolation between the input and output side of the converter. This is commonly done through the use of high-frequency transformers. Hence, these topologies are suitable for applications such as off-line power supplies, etc. Examples of isolated topologies are push-pull, fly back, and forward converters, among others.

1.2. Push-Pull Converter

1.2.1 Basic Converter Operation

The principle configuration of the pulse width modulated push-pull converter is shown in Figure 1-1. The push-pull converter belongs to the family of isolated converters. Galvanic isolation of the secondary is provided by the high-frequency transformer. Note that the transformer turns ratio can be optimized for a given application (step-up or step-down).

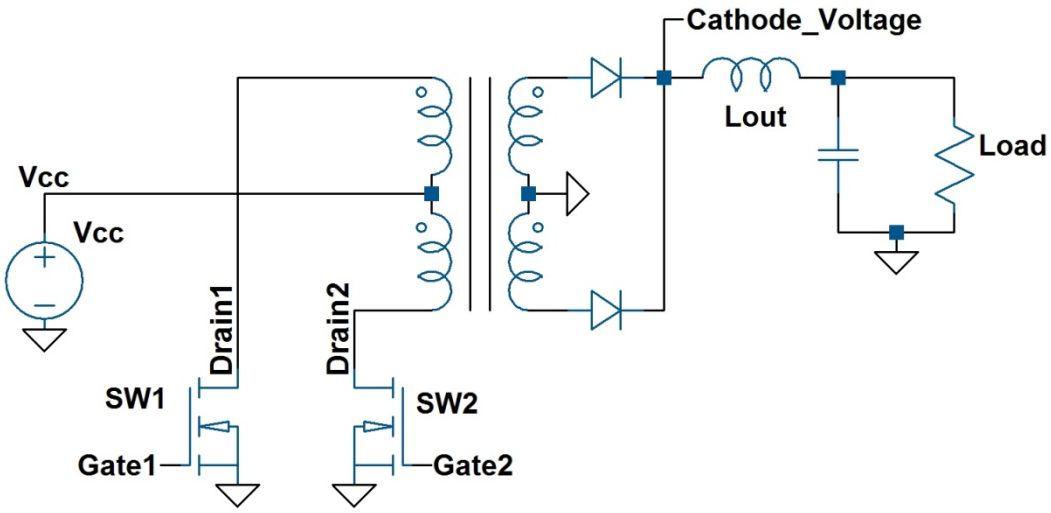

Figure 1-1: Push-Pull Converter

The two power switches operate 180° out of phase—applyi ng rectangular input voltage pulses across the primary windings. Due to the primary winding direction, both switches cannot be turned on instantaneously. An overlap of switch on-time would generate opposing flux in the core, cancelling the primary mutual inductance.

Assuming a low-impedance source, the switch current would be limited only by the transformer leakage inductance (a parameter most often minimized in push-pull transformer design). As such, the switches would quickly fail under the high switching currents.

1.2.2 Switching Characteristics

The switch on-time must be limited to less than 50% of the switching period. Therefore, the three possible switching signals are:

1. SW1 is ON, SW2 is OFF
2. SW1 is OFF, SW2 is ON
3. SW1 is OFF, SW2 is OFF

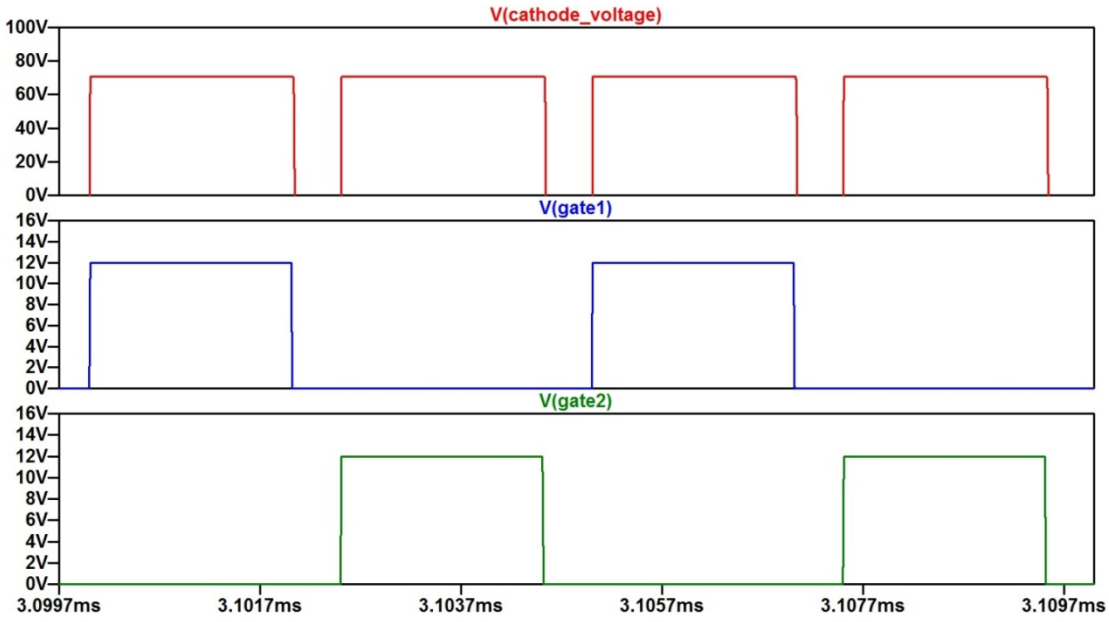

Figure 1-2: Gate and Diode Cathode Voltage

Figure 1-2 typifies the gate signals and the diode cathode voltage on the secondary. The plot indicates the frequency of the rectified transformer output voltage is twice that of the switching frequency. Consequently, the output inductor and output filter capacitor also operate at twice the switching frequency, easing the filtering requirements.

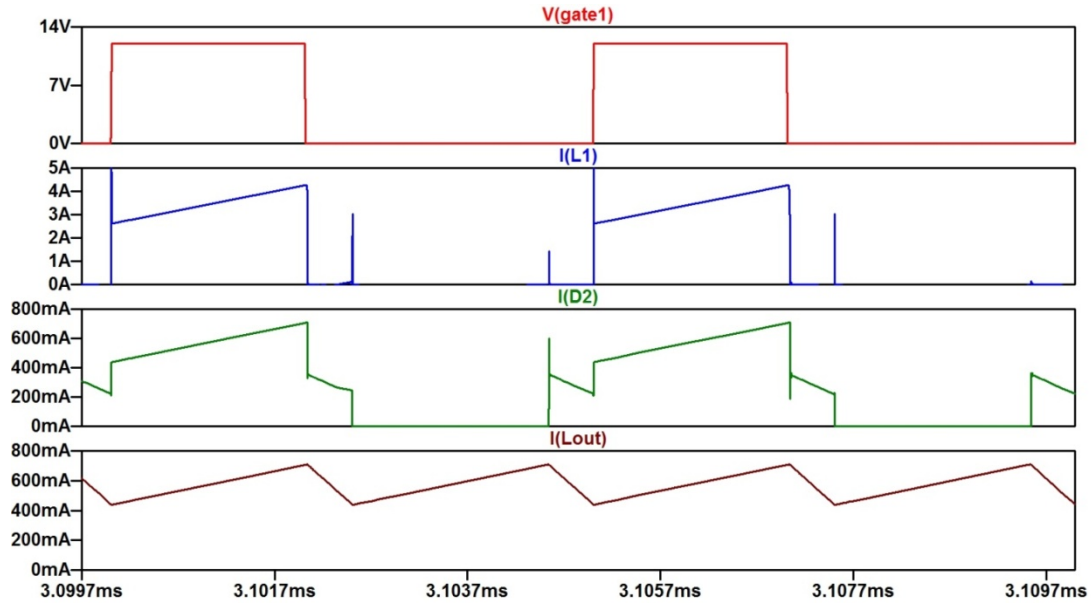

Figure 1-3: Push-Pull Operation

Referring to Figure 1-3, as Switch 1 turns ON, the current in the corresponding primary winding (L1) begins to increase. The magnitude of the current ramp is dependent on the output inductor (Lout) current ramp and the primary-secondary turns ratio.

Prior to Switch 1 turning ON, the diode current (D2) on the secondary is half of the decaying current in the output inductor (Lout). This interval corresponds to the third switching signal possibility—SW1 and SW2 are both off. As such, the inductor current free-wheels through the transformer secondary, splitting equally between the secondary windings. The output inductor current waveform verifies that the output ripple current frequency is twice that of the switching frequency.

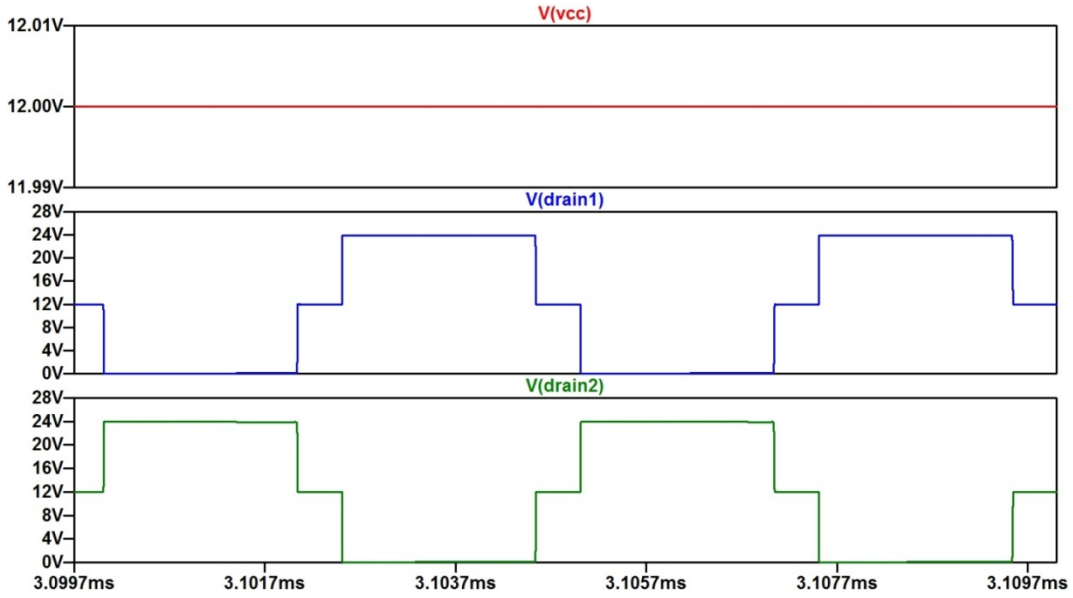

Figure 1-4: Push-Pull Drain Voltages

The off-time switch voltage is shown in Figure 1-4. Since the primaries are wound with the same number of turns, the induced voltages across the windings are equal. During the interval when both switches are off, the drain-source voltage is equal to the supply voltage. However, as Switch 1 turns on, the voltage across Switch 2 becomes the supply voltage plus the induced primary voltage.

The voltage across the winding corresponding to Switch 1 during Switch 1 on-time is equal to the supply voltage. Hence, for the ideal push-pull converter, the maximum switch voltage is equal to twice the supply voltage.

1.2.3 The Effect of Leakage Inductance

The peak voltage stress seen by the push-pull switches is somewhat higher due to the unavoidable presence of leakage inductance. Not all of the magnetic flux generated by the primary windings couples to the secondary windings. This leakage flux leaves the highly permeable core and links back to the winding through the air path.

Figure 1-5 shows a finite element modeling simulation of the leakage flux encountered in an inductor. The coil consists of 114 turns of 14 gauge wire wrapped around Supermalloy core with a relative permeability of 529,095. A 1 KHz 1A sinusoidal current is supplied to the coil.

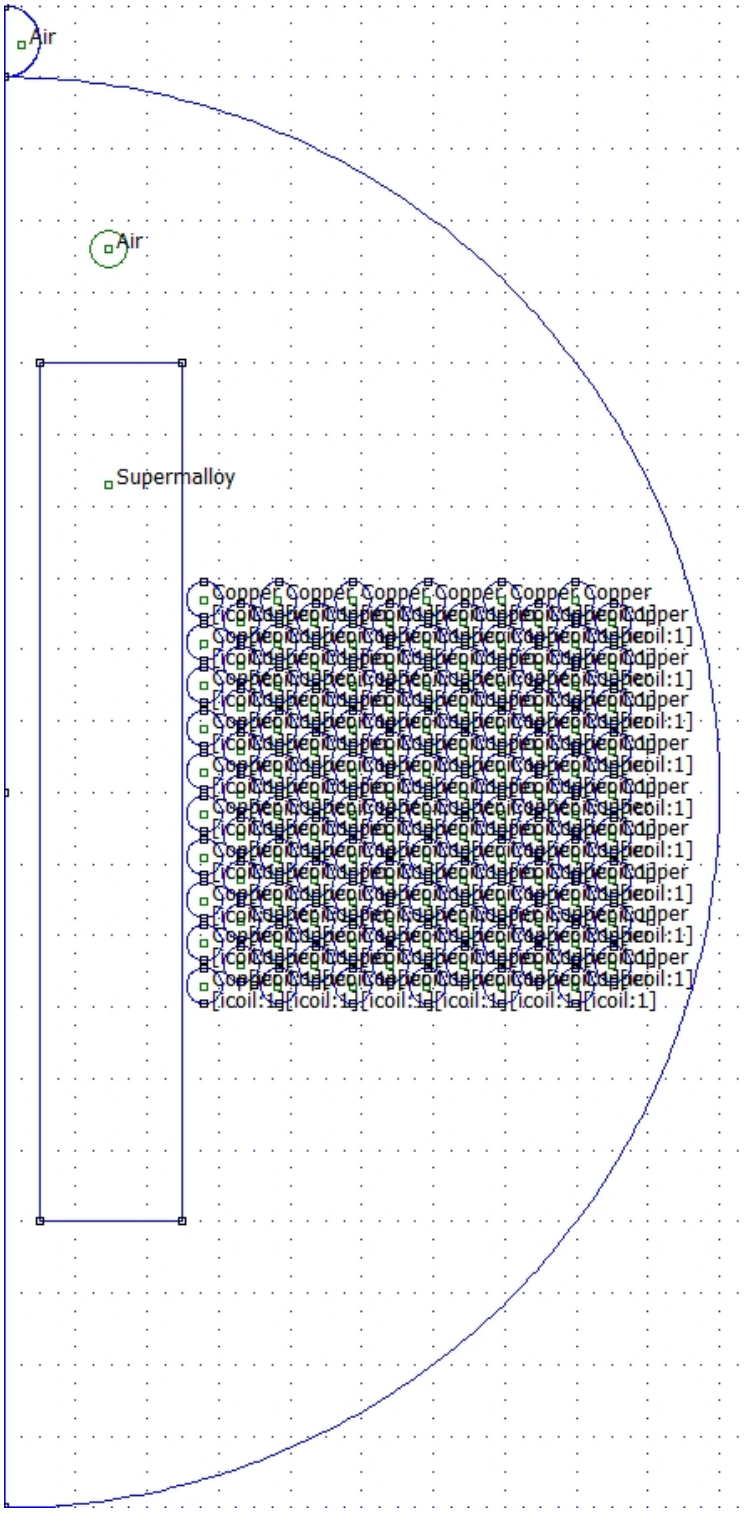

Figure 1-5: FEMM Leakage Flux Simulation

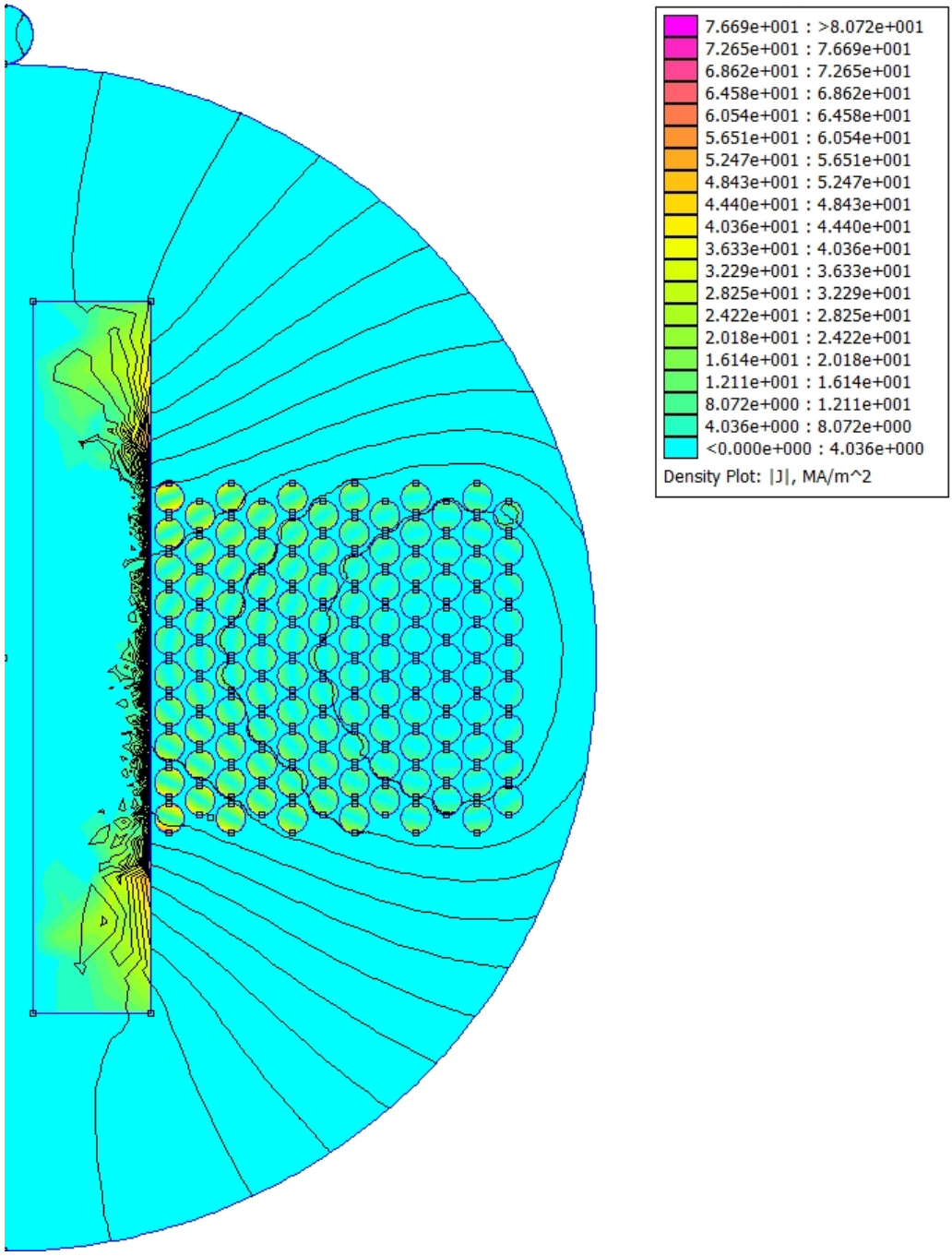

Figure 1-6: Simulation of Absolute Flux Density

The simulation results in Figure 1-6 reveal the flux distribution and the current density (color corresponds to cross-sectional current distribution). From the contour plot of absolute flux density, one can clearly see the contour lines

corresponding to flux not coupled to the core. In the push-pull transformer, the energy stored in the leakage flux cannot be transferred to the secondary windings. The energy (Joules) stored in the leakage inductance is given by:

$$E_{Leakage} = \frac{1}{2} \cdot L_{Leakage} \cdot \left(I_{Pri}\right)^2 \tag{1-1}$$

The voltage spike caused by the leakage inductance occurs as the push-pull switches turn off. For a given current fall time, the amplitude of the voltage spike can be approximated from:

$$V_{Spike} = L_{Leakage} \cdot \frac{\Delta I_{Pri}}{\Delta t} \tag{1-2}$$

1.2.4 Snubber Theory and Design

Assuming that the transformer coupling is greater than 0.96, the leakage spike increases the peak switch voltage by approximately 30% [1]. This significant increase in switch voltage may lead to device breakdown. As such, dissipative circuits (snubbers) are often employed to absorb the leakage energy and reduce switch voltage stresses. Circuit snubbers may be constructed from both passive components (resistors and capacitors) as well as active devices (diodes and switches). Since the snubber circuit must dissipate the energy stored in the leakage inductance, the average power (watts) for a given switching frequency in Hz (F) dissipated by the snubber is:

$$P_{Snubber} = E_{Leakage} \cdot F \tag{1-3}$$

The resistor, capacitor, and diode network in Figure 1-7 (RCD snubber) effectively clamps the leakage spike to a safe level. Most modern semiconductor switches are capable of dissipating overvoltage spikes via avalanche breakdown, provided that the repetitive energy is relatively small. However, the absorbed energy increases the device junction temperature. Snubber circuits allow the leakage energy to be absorbed by resistors instead—reducing the average switch temperature.

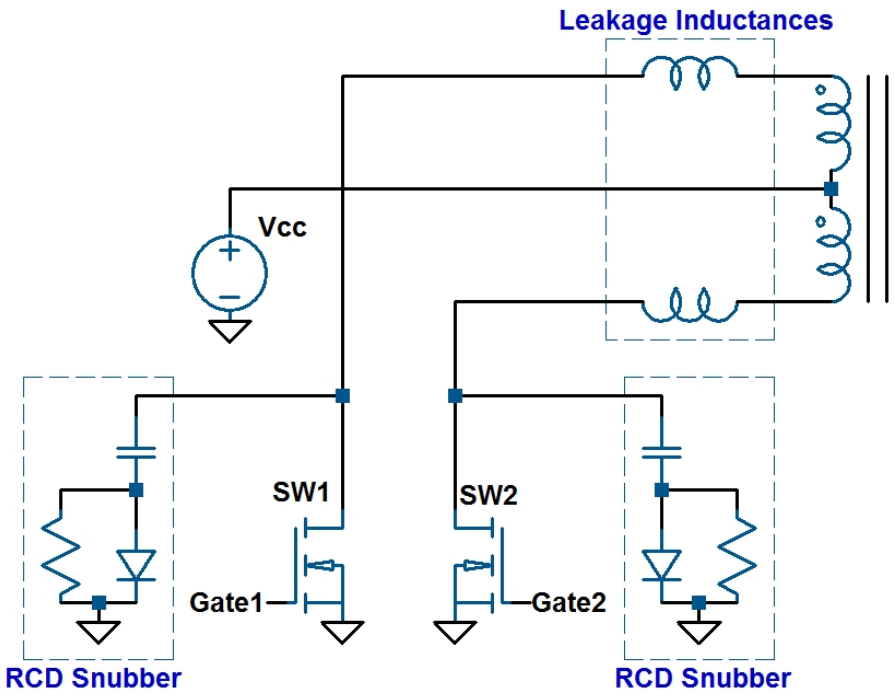

Figure 1-7: RCD Snubber for Push-Pull Primary

Snubber design appears deceptively simple—care must be taken when designing effective circuit snubbers. The extremely fast pulse rise times encountered in switching converters may render sub-optimal designs useless [2].

An excellent example of the pitfalls that plague many snubber designs can be found in Figures 1-8 and 1-9.

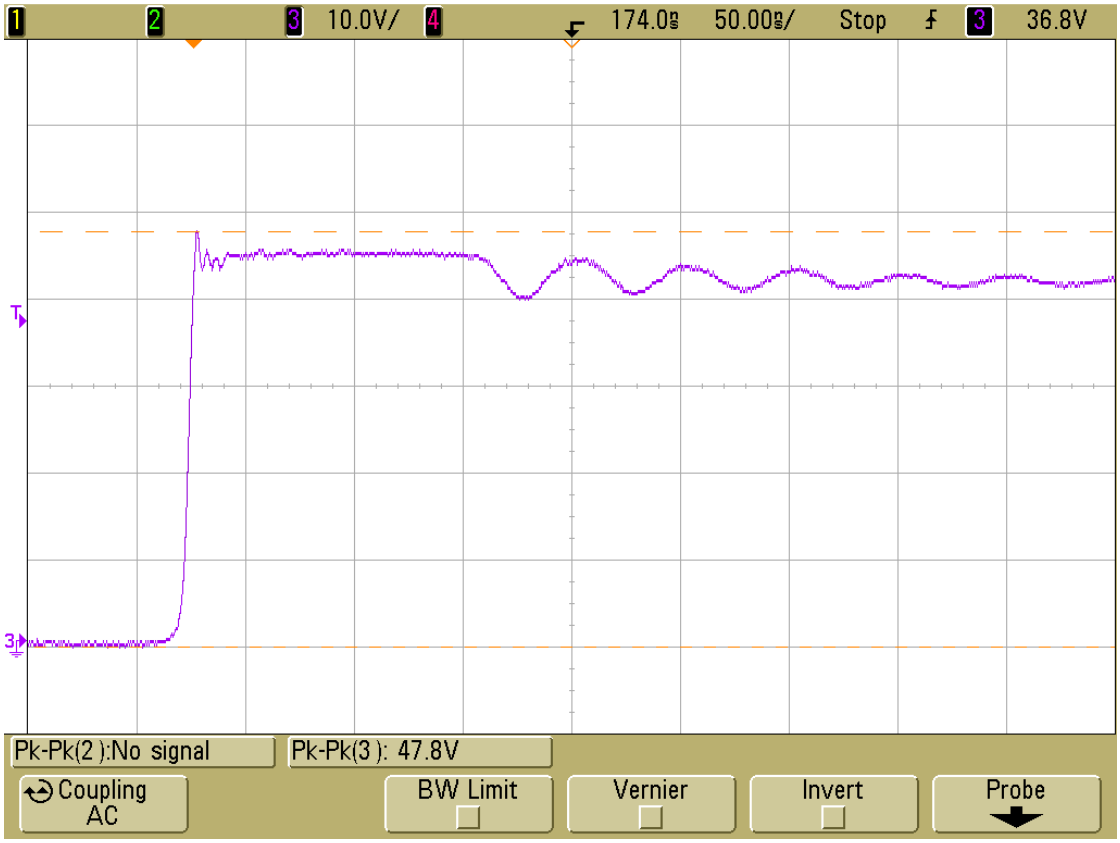

Figure 1-8: RCD Snubber Leakage Spike with Schottky Diode

The first oscilloscope screenshot (shown if Figure 1-8) demonstrates an effective RCD snubber. A low capacitance schottky diode clamps the leakage spike to a paltry 4V above the switch off-state voltage. The sinusoidal oscillation occurring approximately 150ns after the switch turn-off is the result of circuit parasitics oscillating in the primary. The fast rise times present on the switch node voltage dictate the use of a high bandwidth oscilloscope as well as high bandwidth scope probes. Additionally, the scope ground lead impedance cannot be assumed to be negligible at high frequency.

As a result, the scope probe was fitted with a probe jack and soldered to the switch node and ground plane. Lastly, the oscilloscope probe must be correctly compensated to preserve the fidelity of the measured signal.

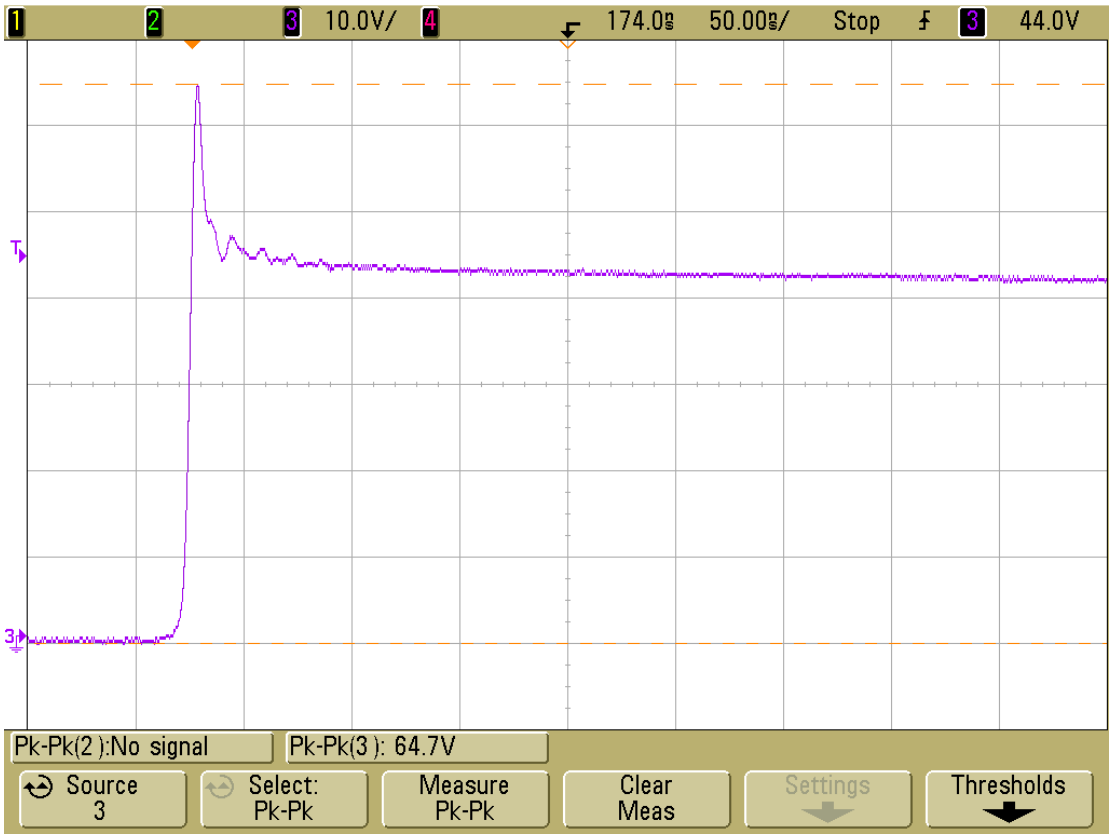

Figure 1-9: RCD Snubber Leakage Spike with Ultrafast PN Diode

Figure 9 reveals that even an “ultrafast” diode may not be fast enough to clamp the leakage spike to a safe level. The leakage spike peaks at 65V—nearly 50% of the nominal switch off-state voltage of 44V. Depending upon the converter specifications, a spike of this amplitude may result in the destruction of the switching device.

1.2.5 Flux Imbalance Problem

In addition to leakage spikes, the push-pull converter is particularly vulnerable to destruction via flux imbalance in the high-frequency transformer [3]. The maximum flux density within the transformer core is given by:

$$B(T)_{max} = \frac{\int V\,dt}{2 \cdot N \cdot A_C} \tag{1-4}$$

Due to the rectangular pulse voltages applied to the push-pull primary windings, the volt-second integral for a push-pull is approximately equal to the supply voltage multiplied by the switch on-time. Any imbalance between the volt-second products of the primary windings will cause the core flux density to drift towards one extreme of the hysteresis curve. The permeability vs. flux density for R-Type ferrite material in Figure 1-10 is typical of high-frequency ferrite materials [4]. As the core material begins to saturate at high flux densities, the effective permeability decreases rapidly. The transformer core's magnetizing inductance will drop precipitously, resulting in dangerously large magnetizing currents. Switching losses will rapidly increase, eventually resulting in failure of the device switching the high magnetizing currents.

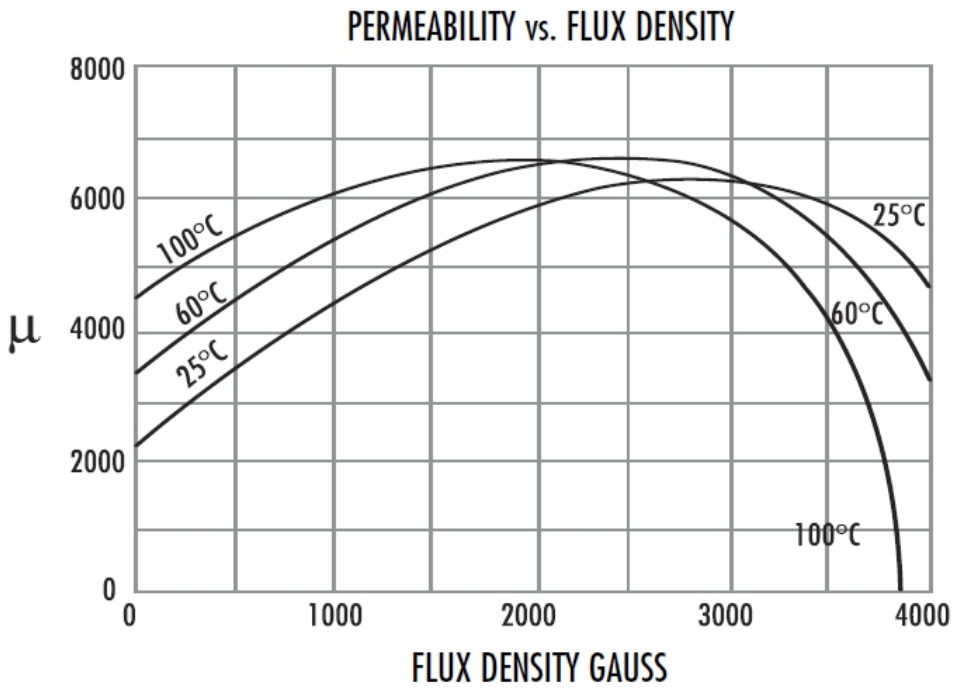

Figure 1-10: R-Type Ferrite Material Characteristics [4]

The positive temperature coefficient of a MOSFET significantly reduces the push-pull converter's sensitivity to any volt-second imbalance [5]. Since the MOSFET drain-source channel appears resistive under sufficient gate-source voltage (Vgs > Vt), the conduction losses can be found from:

$$P_{Loss} = R_{ds} \cdot \left(I_{ds}\right)^2 \tag{1-5}$$

As one of the transformer primary windings drifts towards saturation, the magnetizing current increases dramatically. Power dissipation in the affected MOSFET heats up the device junction, increasing the effective Rds. The voltage drop across the MOSFET increases, reducing the voltage applied to the winding. Care must be taken to ensure that the MOSFET junction temperature stays below the maximum device rating, else the switch will fail.

1.2.6 Voltage-Mode vs. Current Mode Control

The most effective method of avoiding the volt-second imbalance problem is to implement current-mode control in the control loop. Current-mode control regulates the output by monitoring the peak switch current on a pulse by pulse basis. Since the peak switch current is kept constant, the transformer core is not permitted to drift towards saturation. However, the inclusion of current-mode control increases the complexity of the feedback loop. Despite the increased complexity, current-mode control has become the preferred control topology for most DC-DC converters.

Voltage-mode control, the simplest of control topologies, regulates the output by feeding back a portion of the output voltage to the circuit controller. This feedback is compared to a reference voltage and the magnitude of error between the two signals is amplified and applied to the PWM controller. Any deviation of the feedback voltage from the reference voltage will result in a correction of the PWM switching signal. However, many converters (such as the push-pull topology) possess an L-C second-order low-pass filter on the output. The filter introduces a large phase shift and change in gain with respect to frequency and may cause instability of the control loop. For example, any change in the line voltage will result in a delayed change in the PWM signal because the error must *first* appear on the output before being sensed by the error amplifier. The gain and frequency response of the error amplifier and compensation networks must be carefully designed to prevent instability.

Current mode control employs to feedback loops, instead of the single feedback loop in voltage mode control. In addition to sensing the output voltage, current mode control senses the output inductor current directly (most often by sensing the switch current). Any changes in line and load are rapidly corrected by adjusting the PWM signal, which in turn determines the output inductor current. By controlling the inductor current on a cycle by cycle basis, the output inductor may be regarded as a current source. For small-signal analysis, the output filter behaves as a first-order system (due to the presence of the shunt output capacitor). Consequently, error amplifier stabilization becomes a far simpler task.

While current-mode control has become the dominant control architecture, it is not without its limitations. Primarily, the current-mode control loop tends towards instability. The problem arises from the fact that simply controlling the peak inductor current does not necessarily control the average inductor current (and hence the average load current) [6]. Changes in the line and load conditions result in a change of the output voltage. The feedback voltage from the output is sensed by the error amplifier and the controller adjusts the peak inductor current to correct for the error. However, the controller is sensing the peak inductor current rather than the average output current. Unfortunately, the output voltage is proportional to the average output current (and hence the average inductor current) rather than the peak inductor current. As such, the wrong average inductor current is supplied, resulting in an erroneous output voltage. The converter output may oscillate until the correct output voltage is reached. For current-mode converters operating at less than 50% duty cycle, this oscillation

will decay within a finite time [7]. At higher duty cycles, the disturbance in the output voltage caused by the wrong output inductor current will accumulate from cycle to cycle. The slower voltage feedback loop will eventually sense this error, forcing the peak current to increase or decrease in an attempt to minimize the error. Due to the high bandwidth of the current loop, the errors will once again accumulate, resulting in an oscillating instability in the control loop. This instability is often called *subharmonic oscillation*, since it occurs at a frequency lower than the switching frequency. The inherent instability of current mode control can be corrected by adding a small ramp voltage to the inductor current signal. By adding a ramp signal (a technique known as *slope compensation*), the average of the current sense signal depends less on the duty cycle. The ramp voltage prevents the current loop error from accumulating over multiple switching cycles. As such, the lower bandwidth voltage feedback loop can correct the error without unintentionally forcing the converter into subharmonic oscillation. The proportion of ramp signal necessary to prevent instability is dependent on the operating duty cycle. For converters designed to operate over a large range of line and load variation, the current-mode controller should be able to provide variable slope compensation with respect to the PWM duty cycle.

1.2.7 Current-Fed Push-Pull Topology

At high output voltages, the design of the push-pull converter output inductor becomes exceedingly difficult. The output inductor must handle the full load current without saturating, but must also be large enough to ensure

continuous conduction at a specified minimum load. The critical inductance necessary to achieve continuous inductor current is given by:

$$L_C = \frac{V_{OUT} \cdot (1 - D)}{2 \cdot I_{OUT} \cdot F} \tag{1-6}$$

From the above formula, it is clear that a high output voltage and a low minimum output current may necessitate a very large inductance! Additionally, many turns are required to sustain the high output voltage across the inductor. The windings require sufficient margins and insulation to prevent arcing and insulation failure. Parasitic winding capacitance increases with an increased number of turns. This capacitance increases the high frequency noise on the output and may resonate with additional circuit parasitics. If the peak voltage due to resonant ringing is too high, the output rectifier diodes may require snubber circuits to prevent device overvoltage. The aforementioned design challenges may be avoided by removing the output inductor altogether and placing a buck configuration on the input. This type of converter is known as a current-fed converter (Figure 1-11).

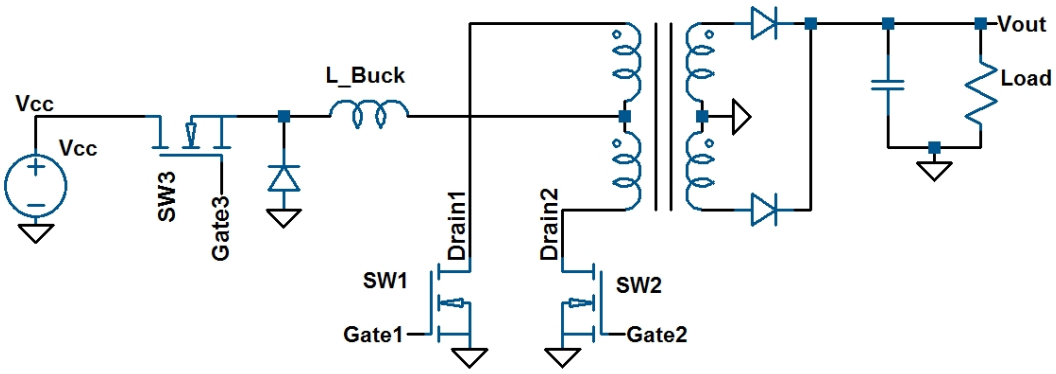

Figure 1-11: Current-Fed Push-Pull Converter

The current-fed push-pull is regulated by PWM control of the buck switch rather than the push-pull switches. Since the buck inductor requires an uninterrupted current path, the push-pull switches are operated slightly over 50% duty cycle. The buck inductor impedance prevents significant switch current when both switches turn on. Additionally, the high inductor impedance prevents flux imbalance problems, as the constant-current nature of the buck inductor prevents high magnetizing currents.

Unfortunately, the addition of the buck stage often decreases the overall converter efficiency. The primary side current must be switched twice: once at the buck input, and once at the push-pull switches. This efficiency penalty may be made relatively small due to the high efficiency inherent to buck converters. Ultimately, the absence of the output inductor makes the current-fed push-pull topology an attractive option for high output voltage converters.

Chapter 2: Resonant Push-Pull Converters

2.1. Switching Losses

Perhaps the largest source of loss within modern DC-DC converters can be attributed to PWM switching of the semiconductor power switches. Ideally, a switching device would be able to transition between a high impedance state to low impedance within an infinitely short duration. Power loss within the switching device would be restricted to conduction losses during the switch ON time. Unfortunately, all power semiconductor devices take a finite time to transition between ON and OFF states. This transition region is characterized by simultaneous current and voltage across the semiconductor switch. The total energy lost during a single switching cycle may be quite small; unfortunately, this loss must be multiplied by the switching frequency in order to calculate the total switching power loss. Often, the switching losses incurred in high frequency converters dwarfs conduction losses by comparison. As such, alternative switching techniques have been employed to minimize or even eliminate switching losses altogether. The technique known as “soft switching” involves commutating the semiconductor device during a zero-current or zero-voltage phase. Without an instantaneous device current or voltage, the instantaneous power loss approaches zero.

2.2. Soft Switching Using Resonance

The most common technique for achieving zero-current or zero-voltage switching is to utilize resonance phenomena.

2.3. Capacitively-Loaded Parallel Resonant Push-Pull Converter

One such topology proposed by Daniel Edry and Sam Ben-Yaakov of the Ben-Gurion University is the Capacitively-Loaded Push-Pull Parallel Resonant Converter [8]. From the circuit in Figure 2-1, one can see that the topology is a current-fed converter. The circuit topology utilizes the parallel resonant “tank” circuit to achieve zero-voltage switching (ZVS) of the push-pull mosfets.

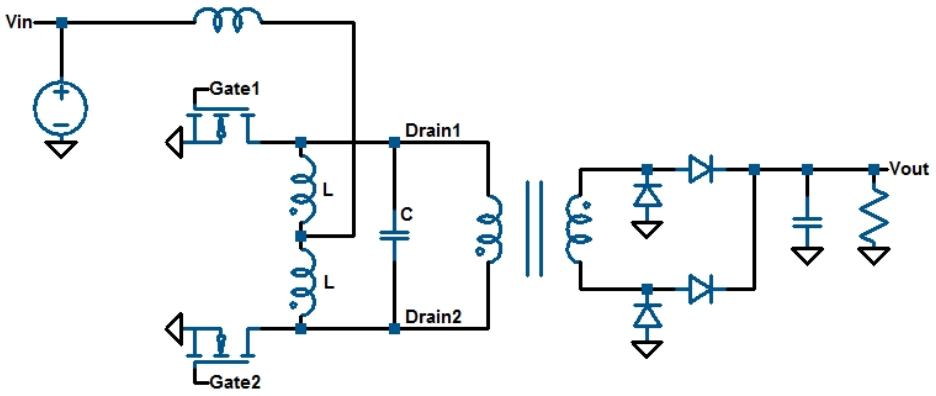

Figure 2-1: Capacitively-Loaded Push-Pull Parallel Resonant Converter

The parallel resonant circuit in Figure 2-1 will experience very high resonant currents as the circuit is being operated near the resonant frequency.

For a known inductance and capacitance (L and C, respectfully), the angular resonant frequency is found by:

$$\omega_0 = \frac{1}{\sqrt{L \cdot C}} \tag{2-1}$$

For a parallel circuit model resistance of R, the parallel circuit quality factor Q is given by:

$$Q = \omega_0 \cdot R \cdot C = \frac{R}{\omega_0 \cdot L} \tag{2-2}$$

Assuming the tank circuit is being driven a current source I, the inductor and capacitor currents are:

$$I_C = I_L = Q \cdot I_{SOURCE} \tag{2-3}$$

The resonant tank circuit possesses very low series resistance. As such, the parallel model resistance will be the reciprocal of the series resistance and consequently very large. A high quality factor implies that the resonant currents may be many times greater than the current supplied by the current source. If the push-pull switches were forced to carry this resonant current, the switch conduction losses would be extremely high. Fortunately, the resonant currents stay locked in the parallel tank circuit for the majority of the switching period. The switches provide the DC current path with a ground return and, ideally, carry the DC input current only.

The push-pull parallel resonant converter (PPRC for short) operates with both switches driven by symmetrical anti-phase drive signals. As such, the

converter achieves regulation via frequency modulation. The PPRC maximum switching frequency occurs at the tank resonant frequency. At the resonant frequency, 100% of the resonant current remains locked in the tank circuit. The push-pull switches conduct only the DC input current. As the converter switching frequency decreases, more current is pulled through the MOSFETs and conduction losses increase.

2.3.1. Modes of Operation

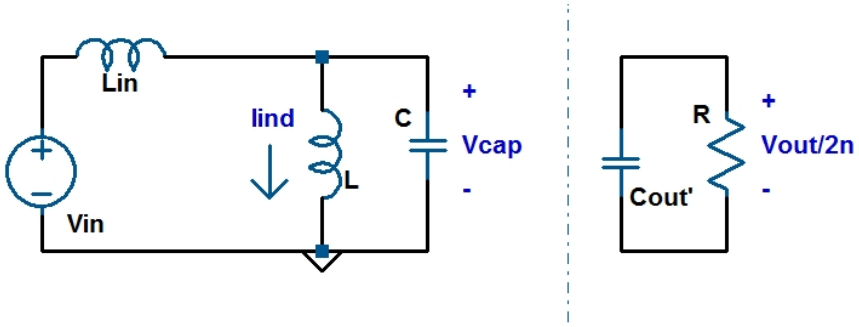

Figure 2-2: Mode 1 - Resonant Rise

The basic PPRC topology possesses four distinct modes of operation. The first mode is characterized by one switch ON and the other OFF (Figure 2-2). For simplicity, the output resistance and capacitance has been reflected to the primary side. The primary resonant capacitor sinusoidally rises from zero volts until just before the output rectifier diodes are biased. During this interval, the output capacitor holds the output voltage constant.

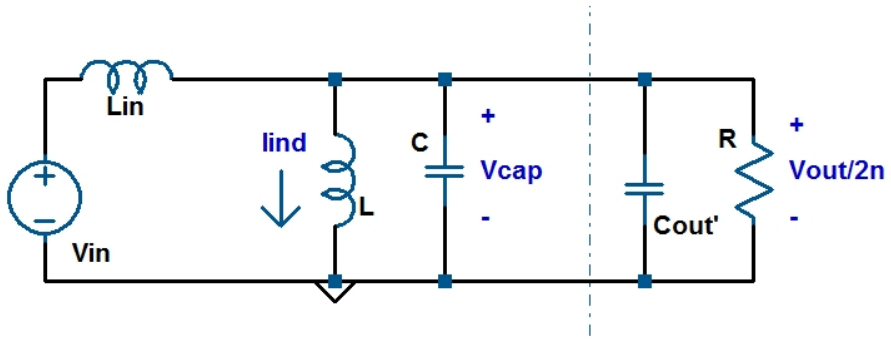

Figure 2-3: Mode 2 - Output Capacitor Charge

The resonant capacitor voltage rises until the output rectifiers are forward biased. The output capacitance begins to charge until the tank energy begins to resonate back to zero volts as illustrated in Figure 2-3. The maximum tank circuit voltage can be approximated by the reflected output voltage. Since the output capacitor holds the output voltage constant (and sets the peak primary side voltage), the topology is aptly named “capacitively-loaded.”

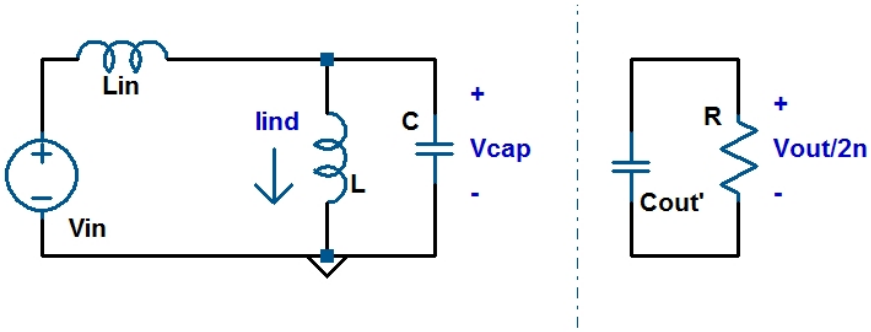

Figure 2-4: Mode 3 - Resonant Fall

The third interval shown in Figure 2-4 is marked by the capacitor voltage resonating down to zero volts. The current-sourcing inductor Lin begins to charge with the full input voltage applied to it.

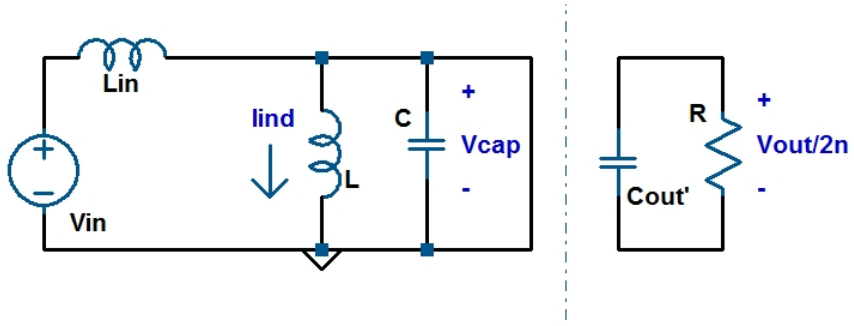

Figure 2-5: Mode 4 - Boost Mode

As the resonant capacitor voltage drops below zero volts, the MOSFET anti-parallel body diode forward biases. With the full input voltage applied to the current-sourcing inductor, Lin begins to charge. During the interval shown in Figure 2-5, the resonant current in the parallel tank circuit passes through the anti-parallel body diode of the OFF MOSFET. Conduction losses in the body diode may be significant. At the end of Mode 4, the push-pull MOSFETs transition states. Both MOSFETs turn ON and OFF with zero drain-source voltage. The energy stored in the current-sourcing inductor during mode 4 empties into the tank circuit in Mode 1 and the switching cycle repeats.

2.3.2. Transfer Function

Intuitively, the PPRC converter will be able to transfer more energy to the output with an increasing Mode 4 interval. The transfer function must be dependent on the ratio of the resonant frequency (f_0) to the switching frequency (f_{SW}). However, the fact that the parallel resonant tank circuit plays an important role in the converter's ability to transfer power is not as obvious. The energy transferred to the load resistance (R_{OUT}) must first be stored in the tank circuit resonance. The characteristic impedance (Z_R) of the parallel tank circuit is given by:

$$Z_R = \sqrt{\frac{L}{C}} \quad (\Omega) \tag{2-4}$$

The ratio of the load resistance to the tank circuit characteristic impedance defines both the maximum power available to the load as well as the division of power between the load and the resonant stored energy. Analysis of the differential equation boundary conditions yields the loaded PPRC topology transfer function:

$$\frac{V_{OUT}}{V_{IN}} = \sqrt{\frac{\pi \cdot R_{OUT}}{2 \cdot Z_R} \cdot \left(\frac{f_0}{f_{SW}} \right)} \tag{2-5}$$

The transfer function assumes that R_{OUT} is the reflected load resistance onto the primary.

2.3.3. Conducted Resonant Current Problem

Unfortunately, the high transfer function afforded by operating the PPRC below the resonant frequency implies that the converter spends a significant amount of time in Mode 4 of operation. During this interval, significant resonant current flows through the anti-parallel body diode. The circuit in Figure 2-1 demonstrates this shortcoming in Figure 2-6.

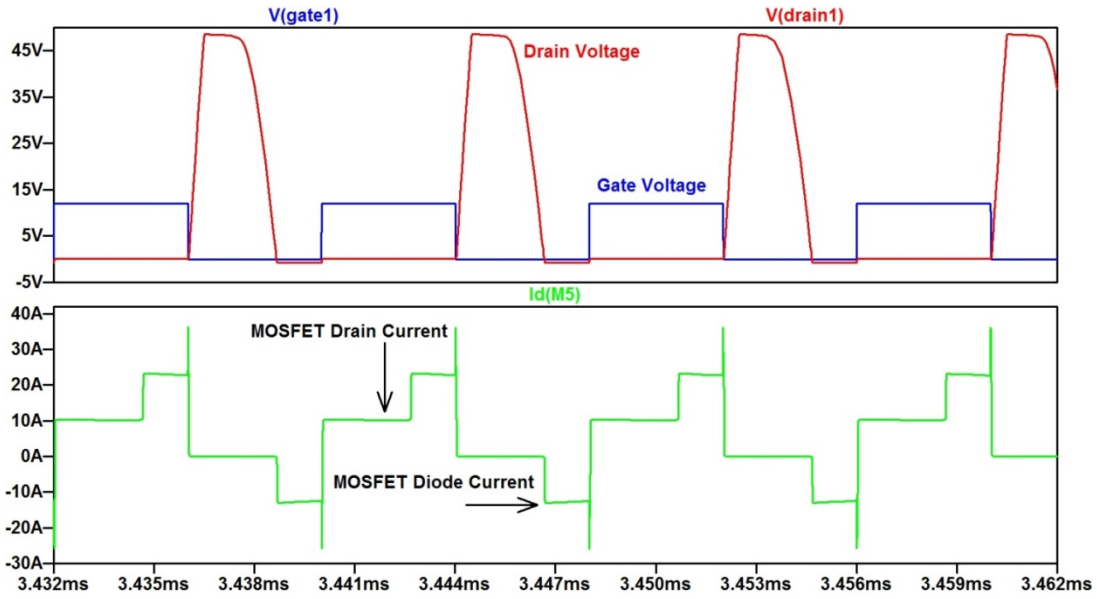

Figure 2-6: CCPR MOSFET Current and Voltage

In order to maintain output regulation over a wide range of line and load variations, the PPRC must tolerate switching operation much lower than the

resonant frequency. As such, conduction losses may relegate the PPRC to lower power designs. The conduction losses could be minimized by forgoing Mode 4 operation altogether and forcing the converter to switch at the resonant frequency—locking the resonant current into the tank circuit. However, doing so would render the PPRC topology unable to regulate the output. The addition of the resonant tank circuit to the push-pull topology greatly minimizes the switching losses. Unfortunately, no regulating push-pull resonant topologies are able to keep the semiconductor switches from conducting the significant resonant currents.

2.4. Boundary-Mode Operation of Parallel-Resonant Push-Pull Topology

The problem, therefore, could be summed up with a single question: how could a parallel resonant push-pull converter simultaneously regulate the output *and* lock the resonant currents into the tank circuit. Before the proposed converter could be regulated, however, the push-pull switching scheme needed to be addressed. One possible solution would to be to provide the push-pull MOSFETs with a switching signal at the calculated resonant frequency. However, the resonant components are likely to vary in exact value with respect to load, temperature, age, etc. The exact resonant frequency will vary, necessitating a closed-loop switching scheme to ensure that the push-pull switch commutation occurs in conjunction with the parallel resonance.

2.5. L-C Oscillator Builder Block

Perhaps the simplest solution would be to allow the resonant circuit to control the switches directly. Surprisingly, this is not a new idea. The earliest L-C oscillators implemented resonance in the feedback path, ensuring that the oscillator switched at the resonant frequency [9]. The cross-coupled L-C MOS oscillator in Figure 2-7 demonstrates this very principle.

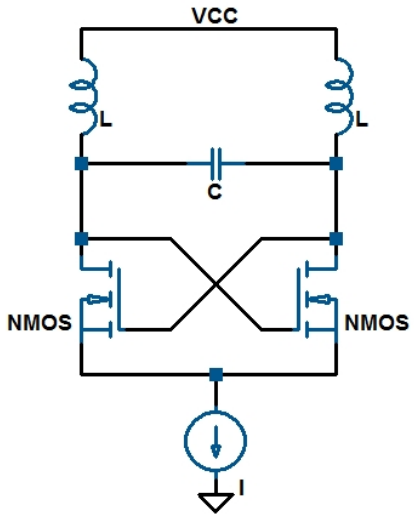

Figure 2-7: Cross-Coupled L-C MOS Oscillator

The L-C oscillator can be broken into two arms with each LC pair setting the frequency of oscillation. Cross-coupling at the drains of the MOS devices applies the oscillating signal to the opposite MOS gate. Assuming the MOS transconductances are equal, the "cross-coupling" produces a negative impedance ($-1/g_m$) at the drain nodes. The criteria for stable oscillation are as follows:

Series R of the resonant inductor:

$$R_s = \frac{2\pi \cdot f \cdot L}{Q_L} \tag{2-6}$$

G_m is given by:

$$gm = \frac{I_D}{\left(V_{GS} - V_T\right)} \tag{2-7}$$

For stable oscillation:

$$\frac{1}{gm} \geq \frac{2\pi\, f \cdot L}{Q_L} \tag{2-8}$$

Generally, the magnitude of the impedance ($1/g_m$) is increased by at least a factor of 2 in order to ensure reliable oscillator start-up [10]. An inductor can be used in place of the current source, so long as the current-sourcing inductor is greater than four times the resonant inductance (Figure 2-8).

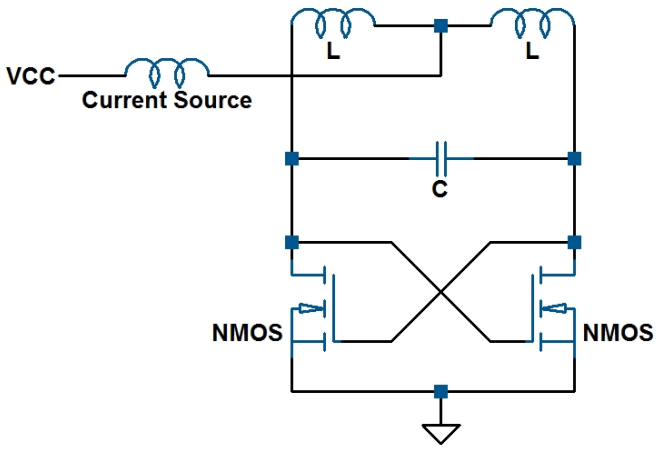

Figure 2-8: Rearranged L-C Oscillator

2.6. Mazzilli Inverter

2.6.1. Theory of Operation

Provided that the criteria for stable oscillation are met, the cross-coupled L-C MOS oscillator can be designed to operate at significant voltages and currents. The MOSFET gate-source voltage, however, can rarely withstand greater than 20V.

One modification to the cross-coupled drain to gate connection is shown in Figure 2-9. The MOSFET gates are pulled up to the supply voltage via a suitable resistor. Cross-coupled diodes prevent drain voltages higher than the supply voltage from exceeding the maximum gate-source voltage. Once the drain voltage drops below the supply voltage, the cross-coupled gate voltage follows the drain voltage resonance.

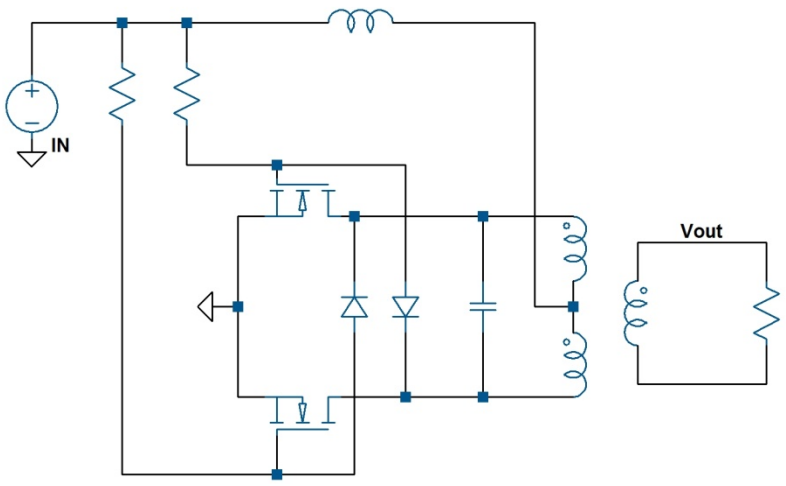

Figure 2-9: Mazzilli Inverter

The Mazzilli inverter in Figure 2-9 essentially combines the L-C cross-coupled parallel resonant oscillator with a center-tapped primary transformer [11]. Surprisingly, the combination unmistakably resembles a current-fed parallel-resonant push-pull topology. By cross-coupling the gate-drain voltages, the inverter oscillates at the L-C resonant frequency. The first mode of the inverter operation can be viewed in Figure 2-10.

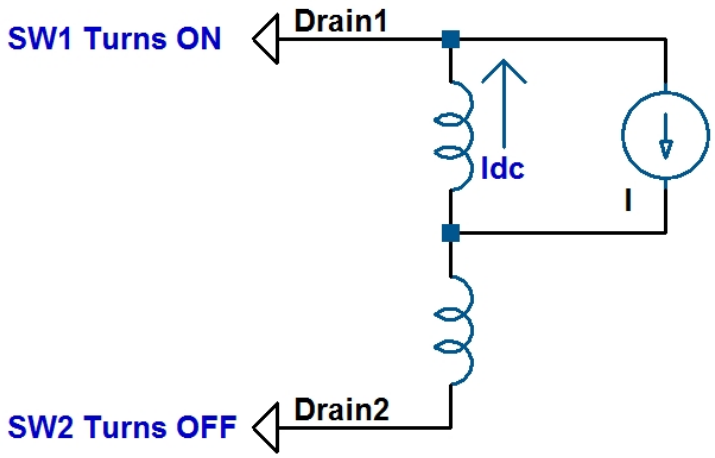

Figure 2-10: Mazzilli Inverter Mode 1 of Operation

Assuming Switch 1 immediately turns ON as Switch 2 turns OFF, the Switch 1 drain provides the DC current ground return path. Both drain voltages are at zero volts, shorting out the discharged resonant capacitor. The energy stored in the resonant tank circuit resides in the peak inductor current. Since the push-pull MOSFETs switched at the instant of zero-capacitor voltage, no resonant current passes through the switches.

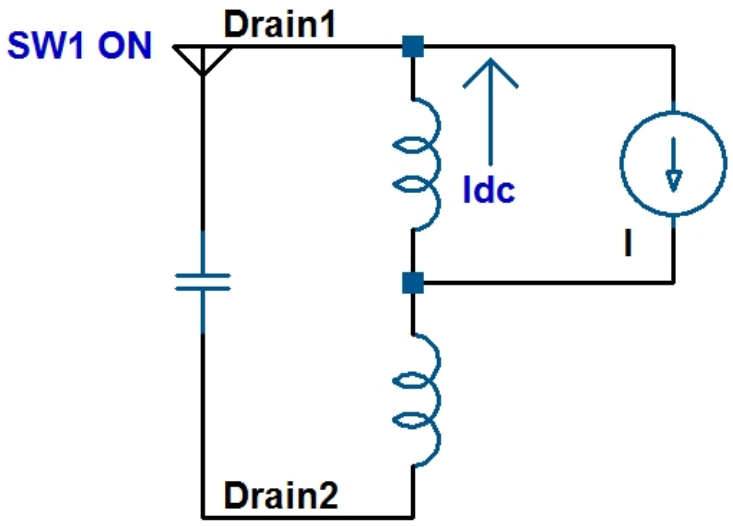

Figure 2-11: Mazzilli Inverter Mode 2 of Operation

With Switch 2 OFF, mode 2 operation (Figure 2-11) is marked by the resonant rise and fall of the resonant capacitor voltage. The resonant inductor current charges the capacitor to the maximum drain voltage midway through the mode 2 interval. At the peak Drain 2 voltage, all of the resonant tank energy is stored in the resonant capacitor. The capacitor/Drain 2 voltage begins the resonant fall back to zero volts—transferring the stored energy into the resonant inductors.

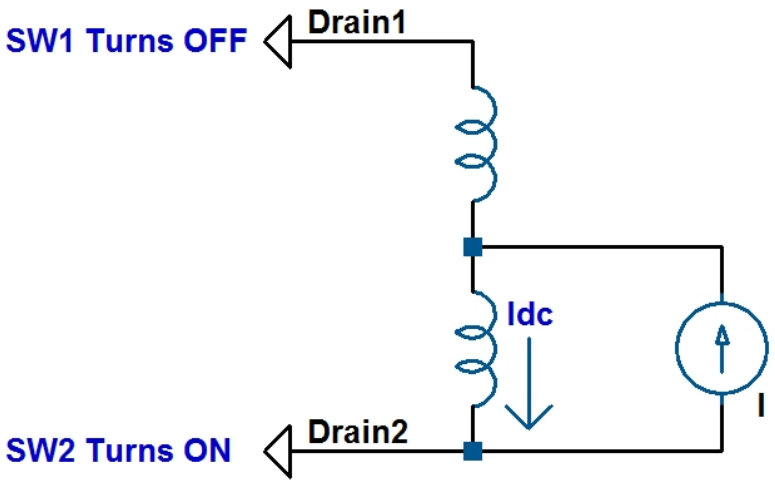

Figure 2-12: Mazzilli Inverter Mode 3 of Operation

Mode 3 depicted in Figure 2-12 occurs as the Drain 2 voltage reaches zero volts. The push-pull mosfets switch, providing the DC current with a path to ground through Switch 2.

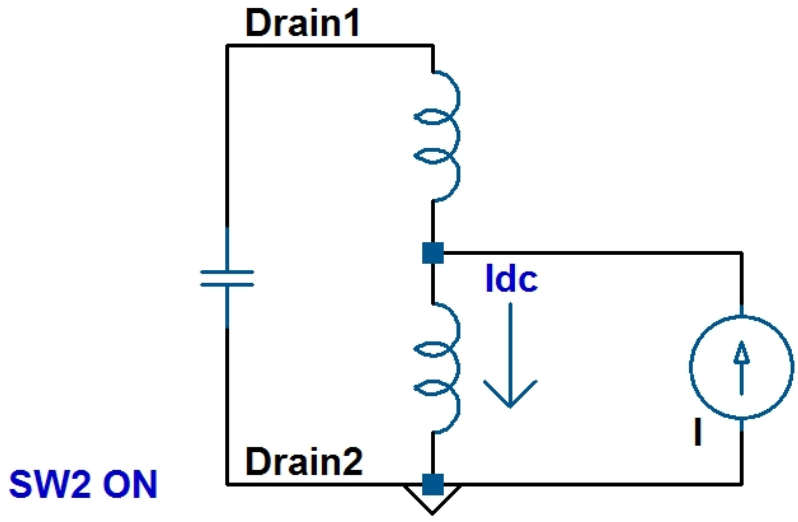

Figure 2-13: Mazzilli Inverter Mode 4 of Operation

The mode 4 interval covers the resonant rise and fall of the Drain 1 voltage as shown in Figure 2-13. Note that the resonant oscillation forces an average of zero volts across the resonant inductors. As such, the transformer primaries will not experience a flux imbalance like the PWM push-pull topology.

2.6.2. Zero-Voltage Switching Characteristics

The MOSFET gate and drain voltages in Figure 2-14 clearly demonstrate true zero-voltage switching. The pull-up resistor and MOSFET gate capacitance lead to a characteristic first-order RC voltage rise at the gate node. The slow MOSFET turn-ON creates an upper-limit for viable switching frequencies. Using low gate-charge MOSFETs, resonant switching frequency is constrained below several hundred KHz. Fortunately, the drain voltage resonant fall means that the slow MOSFET turn-on does not lead to significant loss (as the switching occurs at near-zero voltage).

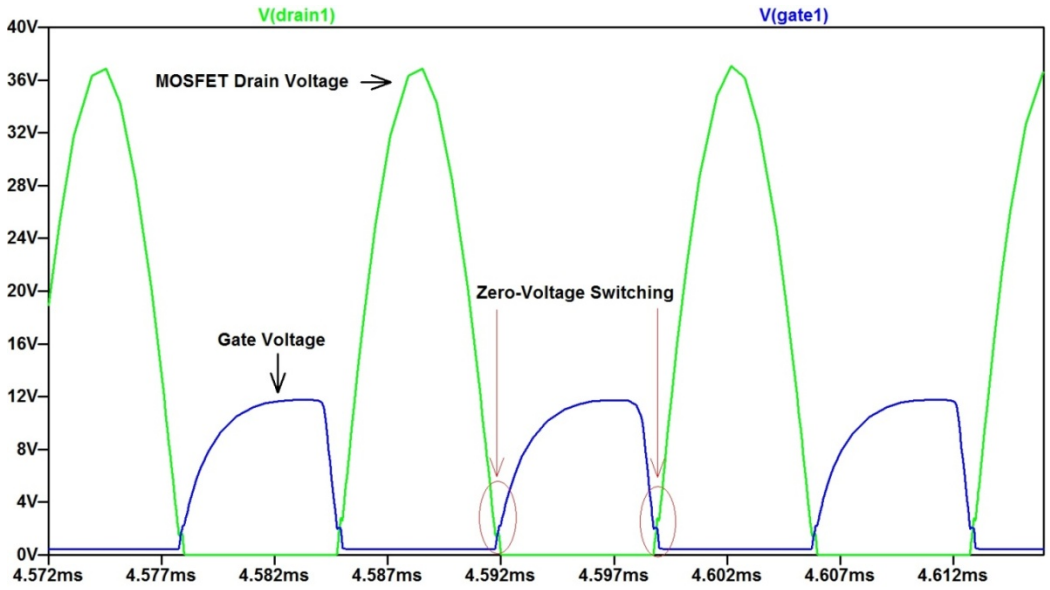

Figure 2-14: Mazzilli Inverter Zero-Voltage Switching

Figure 2-15 provides a more detailed illustration of the switching waveforms. The low impedance of the cross-coupled diode provides a fast switch turn-OFF. The slight discontinuity of the gate voltage during turn-OFF corresponds to the MOSFET “Miller-plateau” region of operation. Again, the near-zero drain-source voltage yields low switching losses.

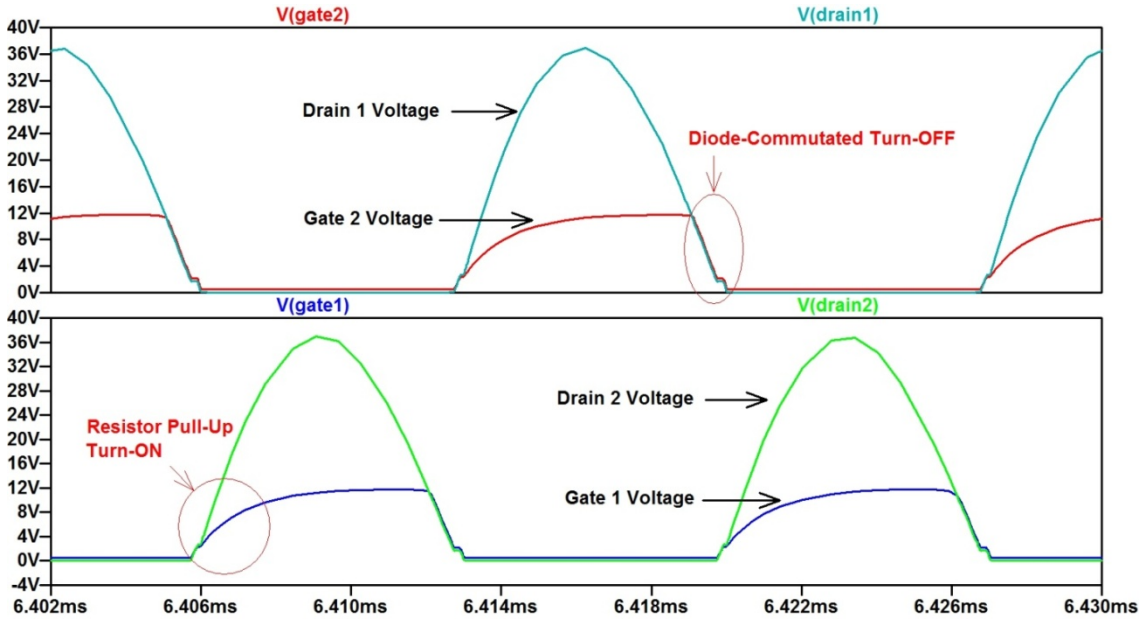

Figure 2-15: Mazzilli Inverter Switching Waveforms

While the MOSFET turn-on time can be reduced by lowering the pull-up resistor value, the power loss in the resistor increases as well. The cross-coupling diode provides a low impedance path to the pull-up resistors. Since the current-fed push-pull topology requires a DC ground return path at all times, one of the push-pull switches is always on. The low impedance path of the cross-coupling diode allows for the full supply voltage to be applied across one of the pull-up resistors.

Total pull-up resistor power dissipation (for both resistors R) due to the low impedance path can be found from:

$$P_R = \frac{\left(V_{DC}\right)^2}{R} \qquad (2\text{-}9)$$

For a sufficiently high gate supply voltage, the pull-up resistor power dissipation may be comparable to the mosfet turn-on losses. As such, the pull-up resistance must not be made so small as to result in excessive power dissipation.

2.6.3. Peak Switch Voltage

The peak drain voltage can be determined by assuming that the average voltage across the current sourcing inductor must be equal to zero. Due to the parallel resonant tank circuit, the OFF-state drain voltages are represented by half sine waves (Figure 2-15). By equating the integral average of the inductor voltage ($V_{Inductor}$) to the DC input voltage (V_{IN}), the peak drain voltage is found to be:

$$V_{Inductor} = \frac{2}{T_{SW}} \cdot \int_{0}^{\frac{T_{SW}}{2}} \frac{V_{Peak} \cdot \sin\left(\frac{2\pi\, t}{T_{SW}}\right)}{2}\, dt = \frac{V_{Peak}}{\pi} = V_{IN} \qquad (2\text{-}10)$$

$$V_{Peak} = \pi \cdot V_{IN} \qquad (2\text{-}11)$$

2.6.4. Transformer Theory

The Mazzilli inverter in Figure 2-9 possesses another interesting modification to the classic L-C MOS oscillator. The resonant inductors are coupled to a secondary winding, generating a sinusoidal voltage on the transformer secondary. Unlike a typical PWM converter transformer, the Mazzilli

transformer must store energy for the resonant circuit as well as transfer power to the secondary.

The primary magnetizing and leakage inductances (Figure 2-16) form the resonant inductance in the parallel resonant circuit. Since the parallel resonance integrates the primary leakage into the tank circuit, the “leakage spikes” present in the PWM push-pull converter do not exist in the Mazzilli inverter. As such, the push-pull switches do not require snubber circuits.

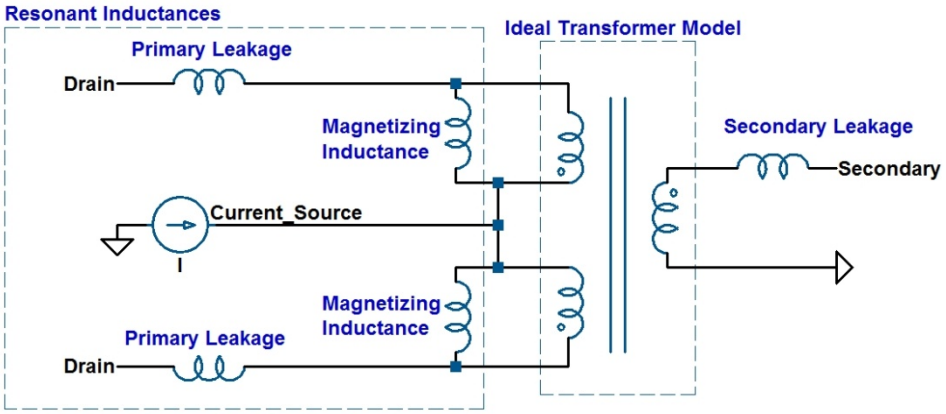

Figure 2-16: Mazzilli Inverter Transformer

2.6.5. Inverter Limitations

The shortcomings inherent to the Mazzilli transformer prove to be the proverbial “thorn in the side” of the Mazzilli inverter topology. Most enclosed high-frequency ferrite cores will yield transformer coupling coefficients greater than 0.9 [12]. As such, the primary magnetizing inductance may be an order of magnitude (or greater) than the leakage inductance. Assuming an unloaded condition and

each primary magnetizing inductance L_{Mag} , the inverter resonant frequency (Hz) may be approximated from:

$$f_{Res} = \frac{1}{2\pi\sqrt{\left(L_{Mag}\right)^{2}\cdot C_{Res}}} \tag{2-12}$$

However, the secondary load impedance will be reflected to the primary side in shunt with the transformer magnetizing inductance. For light to moderate load conditions, the resonant frequency will experience only a moderate change in resonant frequency. Heavy load conditions, however, will shunt the magnetizing inductance, reducing the effective tank circuit resonant inductance. Note that the leakage inductance will not be affected by the transformer load conditions, as the leakage flux is not coupled to the secondary windings. If the magnetizing inductance dwarfs the leakage inductance by an order of magnitude or greater, the resonant tank frequency will increase significantly. Consider the parallel resonant circuit quality factor Q:

$$Q = \omega_0 \cdot R \cdot C = \frac{R}{\omega_0 \cdot L} \tag{2-13}$$

Assuming that the resonant inductance decreases significantly due to a heavily loaded secondary, the circuit quality factor will proportionally increase. The peak parallel resonant currents are Q times the DC input current. Consequently, the resonant currents may increase significantly, leading to very high power loss due to the resonant inductor/capacitor ESR.

During a heavy transformer loading condition, the secondary voltage may be considerably lower than the unloaded secondary voltage. The reduction of magnetizing inductance due to transformer loading decreases the effective voltage applied to the coupled primary voltage. For a known primary voltage, the effectively coupled primary voltage may be found from:

$$V_{Pri,\,coupled} = \frac{L_{Mag}}{L_{Leakage} + L_{Mag}} \cdot V_{Primary} \qquad (2\text{-}14)$$

The voltage divider formed by the transformer leakage and shunted magnetizing inductance reduces the transformer secondary voltage, dramatically reducing the inverter's ability to transfer power during a heavy load condition. Leakage inductance, which severely degrades the PWM push-pull converter's performance, serves to protect the parallel-resonant push-pull topology from a heavy load or a short circuit condition.

The amount of leakage inductance present in the Mazzilli inverter determines the peak resonant currents as well as the maximum inverter power handling. Unfortunately, the leakage inductance present in a transformer depends on many factors (ie. Core geometry, winding geometry, turns ratio, etc). Leakage inductance proves very difficult to calculate prior to transformer construction—as such, it is difficult to design a set amount of leakage into a transformer. External inductance may be added in series with the primary windings in leau of leakage inductance; however, such implementation comes at the cost of two additional inductors.

While the Mazzilli inverter successfully locks the parallel resonant currents into the tank circuit, the absence of sufficient gate drive and the high heavy-load resonant currents relegates the inverter as more of a curiosity than an effective parallel-resonant push-pull topology.

Chapter 3: Novel Current-Fed Boundary-Mode Parallel Resonant Converter

3.1. Proposed Converter Topology

The proposed converter in Figure 3-1 utilizes a Buck topology input to regulate the current into the zero-voltage switching boundary-mode parallel resonant push-pull stage. The high-frequency push-pull transformer incorporated into the parallel-resonant tank circuit (L-Res, C_Res) steps the input voltage up and provides isolation to the secondary side of the converter.

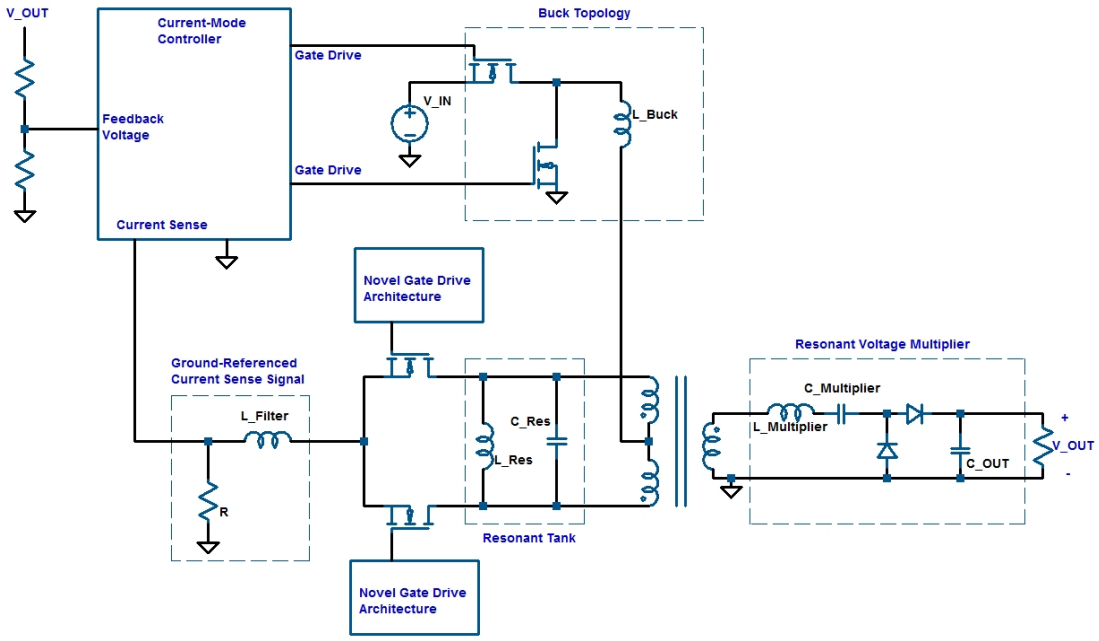

Figure 3-1: Proposed Converter Topology

Additionally, the parallel resonant tank circuit protects the input from an output short circuit condition, allowing the converter to indefinitely sustain an output short. An output resonant voltage multiplier rectifies the secondary voltage

and further steps up the output voltage. Traditionally, the inclusion of multiple stages within a converter degrades the overall converter efficiency; however, the high per-stage efficiency minimizes this effect. The converter implements current-mode control by sensing the parallel resonant push-pull stage output current rather than the buck input inductor current. With a high voltage gain, inherent short-circuit protection, and high overall efficiency, the proposed topology makes an excellent candidate for an isolated high-voltage converter.

3.2. Parallel Resonant Tank Circuit

3.2.1. Discrete Resonant Inductor

The proposed resonant push-pull stage adds an additional resonant inductor (L-Res) to the resonant tank circuit. While the addition of a resonant magnetic component increases the overall converter cost and size, the new resonant tank circuitry greatly benefits the circuit operation. Some of the advantages are: constant resonant frequency operation with respect to output load, stabilization of zero-voltage switching during load transients, and optimization of the tank circuit resonant current during an output short.

3.2.2. Constant Resonant Frequency Switching

In order to obtain the specified advantages of the new tank circuitry, the inductance of the discrete resonant inductor must be less than the primary magnetizing inductance. Since the two primary windings are magnetically coupled, the magnetizing inductance of the series-connected primary windings

must be four times the individual primary winding magnetizing inductances. This series-connected magnetizing inductance is connected in parallel to the discrete resonant inductor. As such, the parallel tank circuit inductance can be found from the familiar equation:

$$L_{Total} = \frac{L_{Res} \cdot \left(2L_{Mag}\right)^2}{L_{Res} + \left(2L_{Mag}\right)^2} \tag{3-1}$$

If the primary magnetizing inductance is equal to the discrete resonant inductance, then the percent change in the effective tank circuit resonant inductance is:

$$\%L_{Total} = \frac{L_{Res} \cdot \left(2 \cdot L_{Res}\right)^2}{L_{Res} + \left(2 \cdot L_{Res}\right)^2} = \frac{4}{5} = 80\% \tag{3-2}$$

The tank circuit resonant frequency (in Hz) is given by:

$$f_{Res} = \frac{1}{2\pi \sqrt{L_{Res} \cdot C_{Res}}} \tag{3-3}$$

By selecting the primary inductance to be equal to the discrete resonant inductor, the 20% reduction in the effective resonant inductance results in an 11.8% increase of the actual resonant frequency. For many designs, the 11.8% change in resonant switching frequency will be tolerable. Note that, if the

designer wishes to reduce the change in actual resonant frequency, the primary inductance needs only to be increased.

Under heavy loading conditions, the reflected output impedance may shunt a significant portion of the magnetizing inductance. Equation 3-1 indicates that the addition of the parallel resonant inductor minimizes the change in resonant frequency as the transformer magnetizing inductance decreases under heavy loads. This assumption precludes that the resonant inductor is less than the transformer primary inductance.

3.2.3. Zero-Voltage Switching Stabilization

The Mazzilli Inverter, a push-pull topology with similar parallel L-C oscillator characteristics, suffers from aberrant switching during load transients. This handicap stems from the fact that the tank circuit resonant magnetizing inductance can be shunted by a reflected load. The sudden change in the resonant circuit potentially may collapse the tank circuit oscillation, leading to a circuit latch-up.

The addition of a discrete parallel resonant inductor prevents a collapse in circuit oscillation by storing its peak energy during the moment of switching commutation (see Figure 3-2).

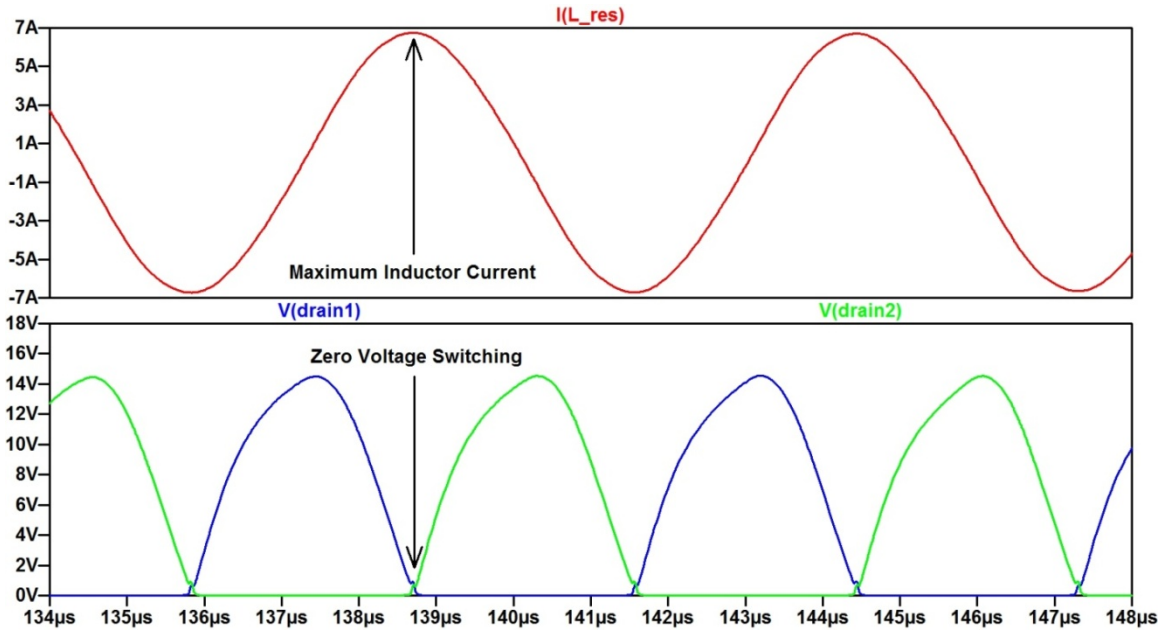

Figure 3-2: Resonant Inductor Current Waveform

Since the resonant inductor current waveform is sinusoidal, the only way for both drain voltages to be zero is if the derivative of the inductor current is zero as well. The zero rate of change of inductor current corresponds to the resonant inductor's peak positive and negative current excursions. Hence, at the moment of switch commutation, all of the resonant tank energy is stored in the resonant inductor. This energy resonates with the tank capacitor during the next switching cycle, causing the necessary resonant rise and fall of the drain voltage. Unlike the Mazzilli Inverter, a load transient will not be able to shunt the inductive resonant energy stored in the discrete inductor (potentially causing a collapse of the circuit resonance).

3.2.4. Short-Circuit Resonant Tank Behavior

Due to the presence of leakage inductance and, in the proposed converter, capacitive ballast from the resonant voltage multiplier, an output short will not be able to completely shunt the primary magnetizing inductance. The change in the loaded magnetizing inductance from the unloaded inductance, however, will still be significant. From the analysis in section 3.2.2, the addition of the discrete resonant inductor was shown to reduce the change in resonant frequency with respect to load by reducing the change in effective resonant inductance. The stabilization of the net inductance serves to also reduce the peak drain voltages experienced during a load transient. A sudden change in the primary inductance may result in excess tank energy appearing as a very high resonant peak drain voltage. If the peak voltage exceeds the MOSFET drain breakdown avalanche energy, the push-pull switches may be destroyed. Fortunately, the resonant capacitor voltage is proportional to the square root of the capacitor energy, and it is unlikely that the transient-induced voltage peaking will be very high. Regardless, without the discrete resonant inductor, the potential for an overvoltage condition exists. The resonant inductor reduces the tank inductance sensitivity to load variations, minimizing any voltage peaking during output transients.

3.3. Novel Cross-Coupled Gate Drive Architecture

3.3.1. Need for High-Performance MOSFET Gate Drive

The high switching frequencies encountered in today's DC-DC converters pose a significant challenge to MOSFET gate drive circuitry. In order to minimize switching losses, MOSFET gate voltages are commutated at the fasted possible speeds. Typical MOSFET gate voltage rise and fall times last no more than tens of nanoseconds.[11] Due to the inherent capacitance of the MOSFET gate, a high frequency gate drive circuit must be able to rapidly sink and source current out of the MOSFET gate connection. For a specified switching interval (Δt_{SW}), the necessary MOSFET gate current can be approximated from:

$$I_{Gate} = C_{Gate} \cdot \frac{\Delta V_{Gate}}{\Delta t_{SW}} \tag{3-4}$$

Note that equation 3-4 does not take into account the non-linear nature of the MOSFET gate capacitance; however, the equation is often a sufficient approximation. In addition to the high slew currents, a high frequency MOSFET gate drive circuit may also need to dissipate a significant amount of power. For a known gate capacitance, bias voltage, and switching frequency, the approximate power (in watts) dissipated by the gate circuitry is given by:

$$P_{SW} = C_{Gate} \cdot F \cdot \left(V_{Gate}\right)^2 \tag{3-5}$$

In addition to strict speed and power handling requirements, gate drive architecture designed for boundary-mode parallel-resonant push-pull topologies

must also be self-oscillating in nature. While the Mazzilli inverter cross-coupled MOSFET gate drive does accomplish boundary-mode operation, it lacks the ability to apply sufficient gate-source voltage during high-frequency operation (see Figure 2-15). As such, the inverter experiences severe switching loss at switching frequencies above 200 – 300 KHZ. Worse still, if the passive gate-drive fails to correctly bias the MOSFETs during a load transient, the Mazzilli inverter may fall out of oscillation. The sub-optimal switching characteristics of the Mazzilli inverter underscore the need for a novel high-power, high frequency MOSFET gate drive architecture.

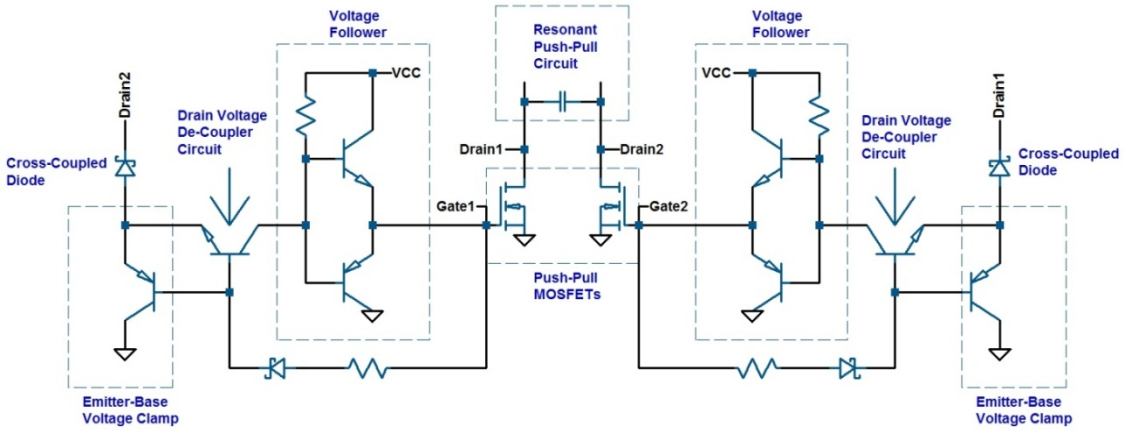

Figure 3-3: Novel Active Gate Drive Architecture

The gate drive topology in Figure 3-3 retains the cross-coupled nature of the parallel resonant L-C oscillator. This MOSFET drain-gate coupling is accomplished via a diode connection, similar to the Mazzilli Inverter. However, the gate pull-up resistors are notably absent. The active gate drive circuitry can be decomposed into several familiar circuit blocks and examined individually.

3.3.2. Voltage Follower

The “totem-pole” NPN-PNP bipolar junction transistor circuitry in Figure 3-3 acts as a simple voltage follower into the push-pull MOSFET gate. While the BJT voltage follower lacks voltage gain, the circuit provides invaluable speed, current gain, and power handling capability. The NPN and PNP transistors share a common Base and Emitter connection. As such, the common emitter voltage is never more than a diode voltage drop away from the common base voltage. The BJT voltage follower, if properly biased, does not saturate. As such, the NPN-PNP totem-pole amplifier possesses a very high usable bandwidth. A NPN-PNP voltage follower composed of signal BJT devices can readily switch at several MHz [13].

The resistor connected from VCC to the voltage follower common base connection serves to pull-up the MOSFET gates, allowing the self-oscillating circuitry to turn on when the VCC voltage is applied.

3.3.3. Drain Voltage De-Coupler Circuitry

While the cross-coupled diode proves to be an effective method of achieving boundary mode operation, the diode’s low Gate-Drain impedance thwarts any attempt to speed up the MOSFET switching. At low resonant drain voltages, the drain-connected cross-coupled diode forces the opposite gate voltage to follow the drain voltage. Due to the relatively slow resonant drain voltage rise and fall, the push-pull MOSFETs are forced to conduct current with

an insufficient gate-source voltage. This undesirable switching condition significantly increases losses at turn-ON and turn-OFF. Unfortunately, the turn-ON losses are especially severe. Since the voltage follower base voltage follows the opposite drain voltage with a diode forward-drop voltage offset, the maximum turn-ON gate voltage is two diode voltage-drops below the rising drain voltage. However, by applying a drain voltage “de-coupling” circuit, the gate voltage turn-ON characteristics are greatly improved.

The “de-coupling” circuit in Figure 3-4 prevents the voltage-follower base-voltage from following the cross-coupled diode voltage during the MOSFET turn-ON interval.

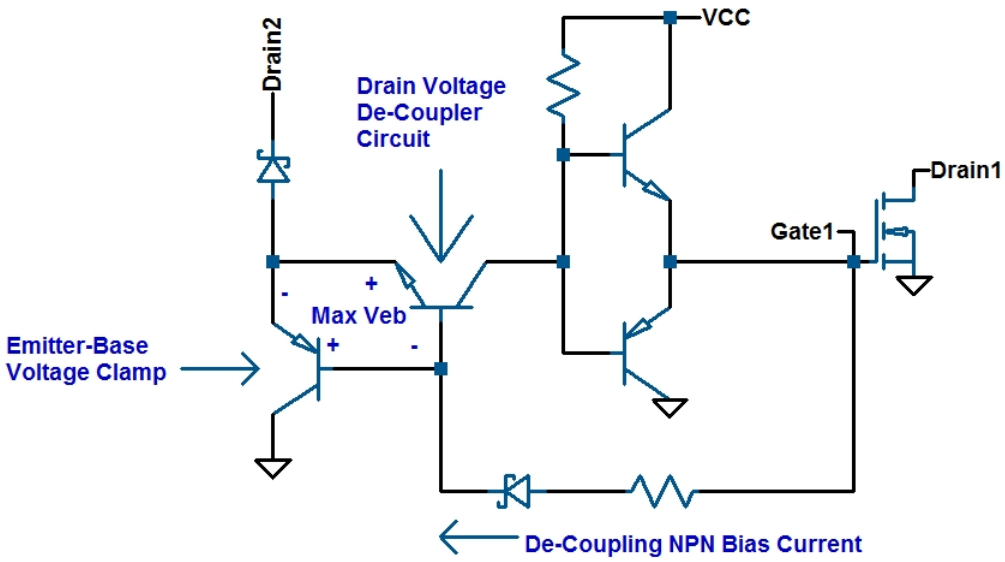

Figure3-4: Drain Voltage De-Coupling Circuit

Prior to the MOSFET turn-On, the gate-source voltage stays low (<1.5 V). As the opposite MOSFET’s drain voltage begins the resonant rise, the anode end of the cross-coupled diode voltage follows as well. However, the low gate-source

MOSFET voltage prevents the base of the drain voltage de-coupling NPN transistor from receiving current. The NPN stays OFF, allowing the voltage follower pull-up resistor to quickly turn the MOSFET ON. Due to the fast voltage rise times, the de-coupling NPN emitter-base voltage may be pulled too high. The maximum emitter-base voltage for a switching BJT is limited to approximately 6 V [14]. A PNP BJT device is connected to the base and emitter terminals of the de-coupling NPN, preventing the NPN Emitter-Base voltage from exceeding 0.55 V. The Emitter-Base voltage clamp PNP diode also prevents the de-coupling NPN from saturating, ensuring that the de-coupling circuitry can operate at very high switching speeds.

3.3.4. Simulated Switching Characteristics

The offset voltage problems that necessitate the de-coupling circuit during turn-ON actually benefit the switching characteristics during turn-OFF. As the opposite drain voltage falls to zero volts, the cross-coupled diode and the voltage follower force the MOSFET gate voltage to be two diode forward voltage drops above the resonant fall voltage. This prevents the MOSFET from experiencing insufficient gate-source voltage prior to the boundary-mode switching commutation. The simulated MOSFET gate and drain voltages during turn-ON and turn-OFF are shown in Figure 3-5.

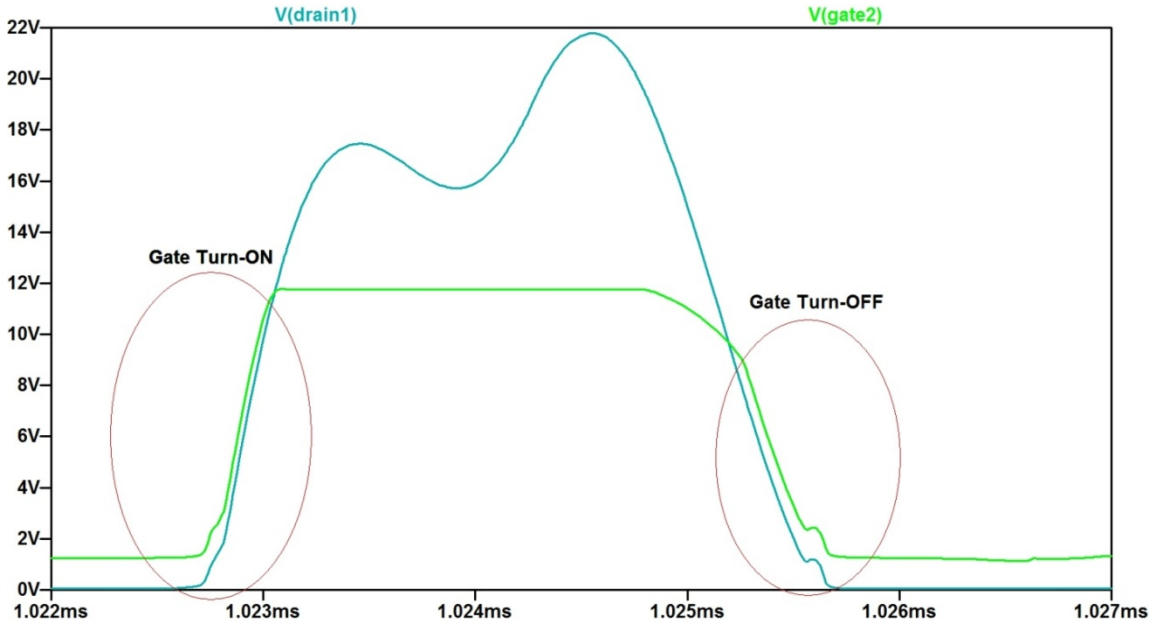

Figure 3-5: MOSFET Gate and Drain Voltages

The gate voltage waveform in Figure 3-5, while certainly not a rectangular pulse, is sufficient to provide very low loss. Note that the drain voltage waveform corresponds to the opposite MOSFET and not the gated MOSFET. For boundary-mode operation of the resonant push-pull converter, both MOSFET drain voltages reach zero volts at the same time. Therefore, one can verify that the MOSFET does achieve zero-voltage switching at turn-ON and turn-OFF.

Quiescent power loss within the gate drive circuitry is extremely low due to the lack of heavy BJT biasing. The only significant power dissipation occurs as the voltage follower sinks and sources the MOSFET gate current. Since this power is intrinsic to the MOSFET gate biasing, the only means of reducing this power dissipation is to use low gate charge MOSFETs and/or low threshold MOSFETS.

Ultimately, the novel gate drive architecture proves effective at implementing efficient zero-voltage switching for the boundary-mode parallel resonant push-pull topology.

3.4. Current Mode Control

For the standard current-fed push-pull converter, current mode control adjusts the Buck topology PWM switching in order to regulate the input inductor current. This implementation of current-mode control, however, is complicated by the presence of the boundary-mode parallel resonant push-pull circuit. The parallel resonant push-pull stage generates a sinusoidal ripple current due to the boundary-mode resonant switching. As the input Buck stage and parallel-resonant push-pull stage are in series, superposition states that the sinusoidal ripple current will be superimposed on the input inductor current ramp. The distorted current waveform may contain significant frequency content unrelated to the inductor current ramp. Consequently, the input inductor current signal cannot be used to implement current-mode control.

The parallel resonant tank circuit, by definition, must act as a second-order parallel L-C filter. Assuming that the circuit quality factor is high, input frequencies above and below the resonant frequency will be attenuated on the output. The parallel resonant filter can be used to remove much of the Buck inductor current ramp from the output of the boundary-mode parallel resonant push-pull stage. This inherent filtering is used in Figure 3-1 to obtain a ground-referenced current-sense signal via an additional inductor and current-sense

resistor after the push-pull stage. The simulated current-sense signal in Figure 3-6 contains only a small amount of the Buck inductor ramp.

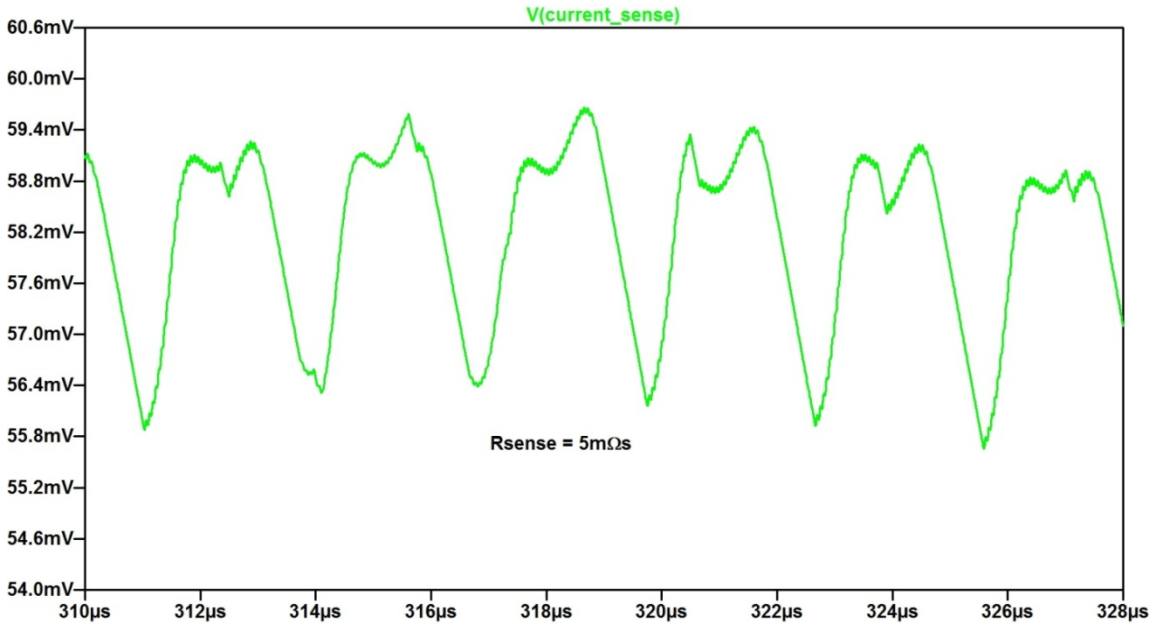

Figure 3-6: Ground-Referenced Current-Mode Signal

If the magnitude of the superimposed Buck inductor current ramp on the current-mode signal is too high, the PWM controller may begin to switch erratically. Fortunately, the high average-to peak ratio of the ground-referenced current sense signal affords sufficient tolerance to most current-fed Buck topologies.

Since the converter generates a single ground-referenced current-sense signal, most commercially available current-mode PWM controllers may be chosen to provide the closed-loop control architecture. The wide selection of commercially available controllers lowers the overall converter cost as no novel control scheme needs to be developed.

Additionally, commercial controller ICs may possess some of the necessary power supply logic (i.e. soft-start, synchronization, multi-phase capability, digital interface, etc.), further simplifying the converter design process.

3.5. Resonant Voltage Multiplier Output

3.5.1. Charge-Pump Based Step-Up Rectification

Voltage multiplier circuits are commonly used to efficiently obtain a high DC output voltage from an AC voltage source. The dual rectification/step-up properties of voltage multipliers are particularly useful in isolated topologies, as the step-up transformer requires a less severe turns-ratio.

3.5.2. The Voltage Doubler Circuit

The voltage doubler circuit in Figure 3-7 simultaneously rectifies the AC input voltage and charges the output capacitor (C_OUT) to two times the peak AC input voltage. The diode polarity in Figure 3-7 indicates that the output must be a positive voltage with respect to ground. Since the input voltage alternates between positive and negative amplitudes, the voltage doubler circuit operation can be deduced from examining the circuit operation with a negative and positive input voltage, respectfully. The negative input voltage in Figure 3-8 forward biases diode D1 and reverse biases diode D2.

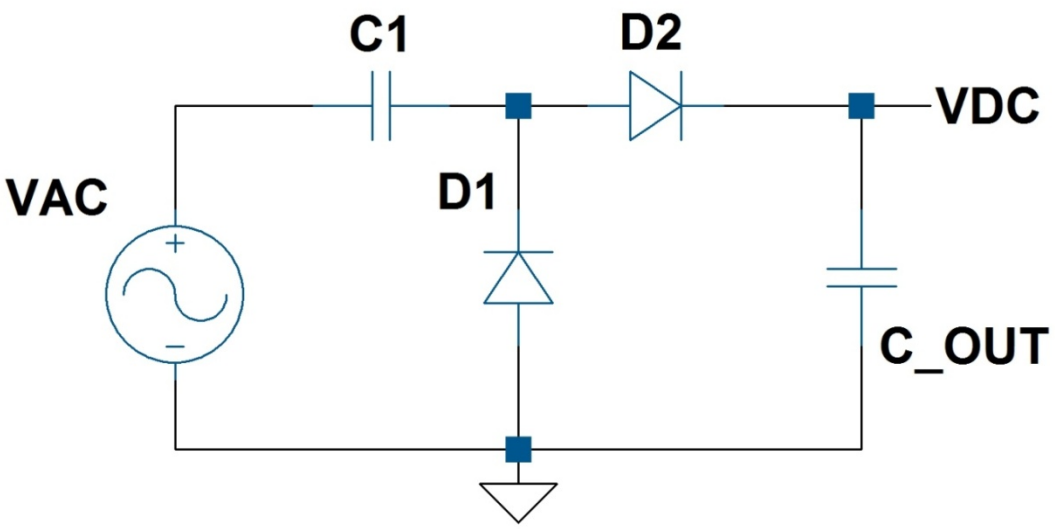

Figure 3-7: Voltage Doubler Circuit

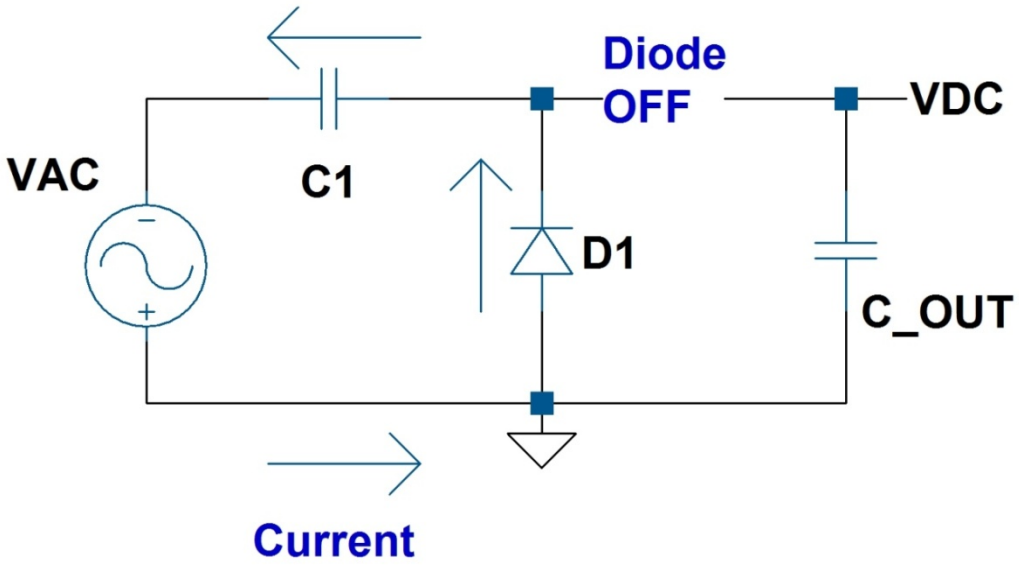

Figure 3-8: Voltage Doubler with Negative Input Voltage

With D1 forward biased, the output side of capacitor C1 is held near ground potential. Assuming a low impedance source, the input side of capacitor C1 charges to a peak negative input voltage. Diode D2 must withstand a peak reverse voltage of the output voltage plus the peak input voltage.

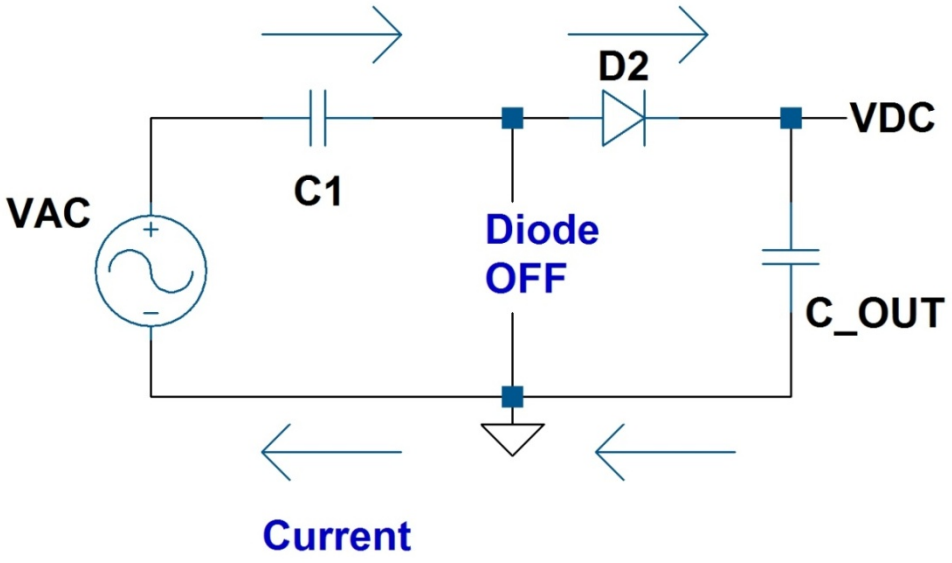

Figure 3-9: Voltage Doubler with Positive Input Voltage

The charge stored on the capacitor C1 is pushed onto the output as the input voltage transitions to a positive voltage in Figure 3-9. This charge-pump action raises the output voltage to twice the peak input voltage. Consequently, diode D1 must withstand a peak reverse voltage of twice the peak input voltage as well.

3.5.3. Resonant Voltage Multiplier

Transformer leakage inductance may be minimized by careful design; however, the presence of leakage inductance can never truly be eliminated. The energy stored in the transformer secondary leakage inductance can (and often does) resonate with circuit parasitics. Resonant voltage peaking may result in overvoltage of the secondary side rectifiers in isolated DC-DC converters. However, in Figure 3-10, the parasitic leakage inductance can be successfully integrated into the resonant voltage multiplier.

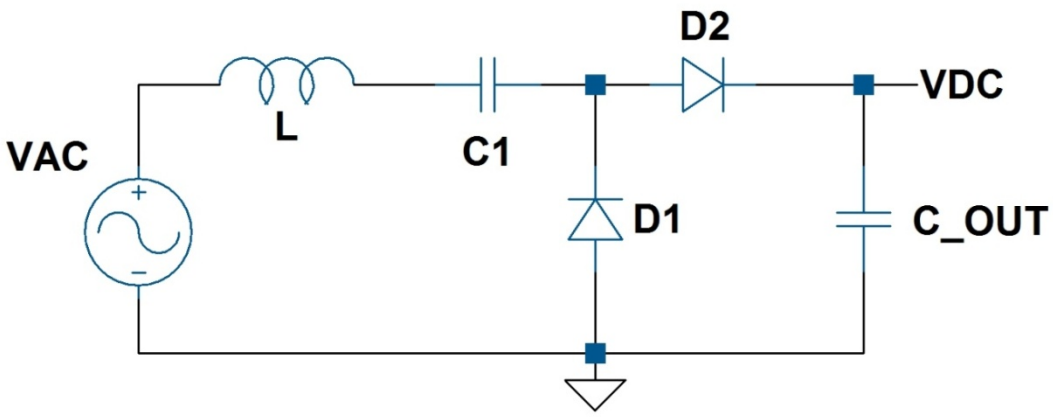

Figure 3-10: Series Resonant Voltage Multiplier

The series resonance of the transformer secondary leakage inductance with the voltage multiplier AC capacitor C1 leads to resonant voltage peaking provided that the AC input voltage is near the series resonant frequency. For a given series quality factor of Q, the peak AC capacitor voltage is given by:

$$V_{CAP} = Q_{Series} \times V_{AC} \quad (3\text{-}6)$$

Note that the series resonant circuit charges every half-cycle. Thus, the resonant voltage multiplier resonates with twice the AC input frequency. Fortunately, a higher resonant frequency results in a smaller necessary inductance and capacitance.

By charging the AC capacitor to the peak series resonant voltage, the overall voltage gain of the resonant voltage multiplier may be greatly increased. Too much resonant peaking, however, may lead to erratic circuit behavior in the boundary-mode parallel resonant push-pull converter. While the leakage inductance is not coupled to the transformer core, the resonant current through the secondary windings is reflected onto the primary current waveform. The reflected secondary resonant currents, if close to the magnitude of the primary tank resonant currents, may distort the drain resonant waveforms. Since the boundary-mode gate drive circuitry relies on the drain voltage resonance to commutate the push-pull circuitry, the distortion may cause erratic switching. The amount of tolerable drain distortion depends upon a myriad of factors, as the drain resonance reflects the composite resonance of all reactive components present in the converter. Fortunately, the very fact that the drain distortion is nearly impossible to quantify means that a wide range of secondary series resonance inductor and capacitor values will suffice. Generally, the secondary side resonant frequency should be 20% higher or more than the primary resonant frequency to prevent excessive drain distortion while still reaping the

resonant voltage gain. Hardware testing will be the only way to ensure that the resonant voltage multiplier components will perform as desired.

3.6. Converter Design

3.6.1. The First Step—Requirements

It goes without saying that the first challenge facing a new design is deciding where to begin. Each component comprising the converter must correctly execute a specific function, else the entire converter will not work. The first step in the design process is analogous to taking a long walk; one must decide first where one is going. As such, the converter design began with determining the necessary requirements. The proposed converter excels in step-up applications; therefore, the proposed design would be a step-up DC-DC converter. While many applications for step-up converters exist, one particular application appeared especially interesting. Renewable energy systems often rely on battery energy storage and/or low voltage energy sources (i.e. photovoltaic panels). In order to efficiently utilize these energy sources, however, the operating voltages often need to be increased. One particularly common application involves stepping up 12 VDC from a battery to 170 – 180 VDC for a PWM-based inverter. The 170 VDC voltage is chopped and filtered to provide loads with 120 V RMS AC voltage. Without question, the proposed converter could serve to step-up battery voltage to 170 – 180 VDC. However, if the converter could achieve very high efficiency (85 – 90%) at a medium power level (100 W), then the proposed topology would prove to be a viable design choice.

With these preliminary criteria in mind, the converter design process began to unfold.

3.6.2. The Current-Mode Controller

The current-mode controller acts as the brains for the converter, handling the myriad digital and analog circuit operations needed to maintain output voltage regulation. Since the proposed topology only requires one ground-referenced current-sense signal to implement current-mode control, the plurality of suitable current-mode controllers proved almost overwhelming at first. Eventually, one controller was chosen—the Linear Technology LTC3862 Multi-Phase Current-Mode Step-Up DC-DC Controller in Figure 3-11 [15].

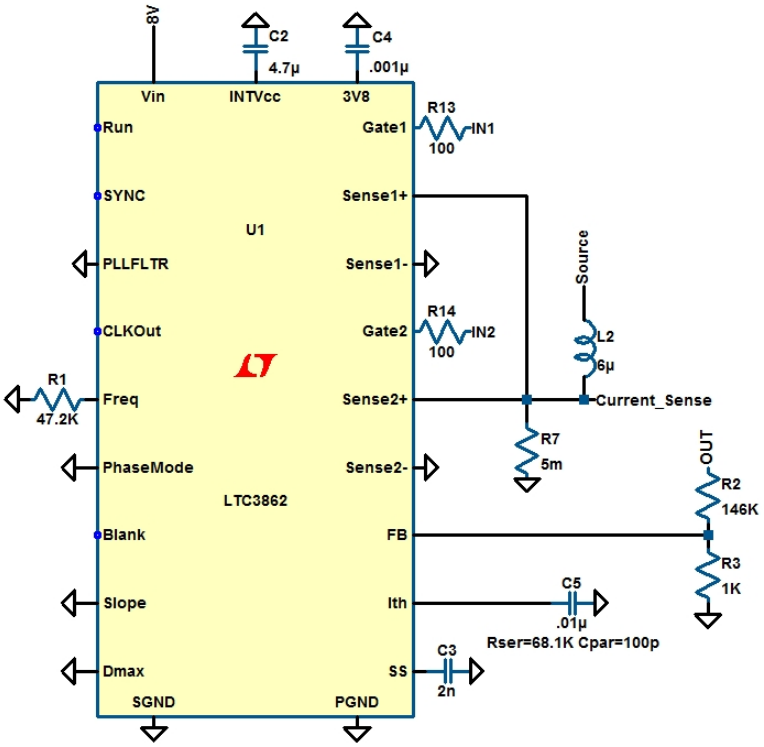

Figure 3-11: LTC3862 Multi-Phase Current-Mode Controller [15]

The controller provides two anti-phase PWM outputs, allowing the proposed converter to implement multi-phase operation of the Buck topology inputs. By operating the Buck inputs 180°out of phase, the effective input switching frequency doubles. An individual Buck input switching frequency of 300 KHz results in an impressive 600 KHz input ripple frequency. Additionally, the two inputs only have to handle half of the input power, allowing for smaller Buck inductors, smaller MOSFETS, and reduced filtering requirements.

The multi-phase operation also reduces the effective distortion seen on the current-sense signal as the parallel-resonant tank circuit filters the higher effective switching noise more efficiently.

3.6.3. The Buck Topology Input

Since the current-mode controller does not drive the MOSFET gates directly, the controller PWM signal outputs connect to two LTC4442 High Speed Synchronous N-Channel MOSFET Drivers shown in Figure 3-12 [16]. The Buck topology input stage benefits greatly from the synchronous operation since the MOSFET conduction losses are much less than the comparable Schottky diode conduction losses. Fortunately, the low DC input voltage allows for the use of low-gate charge, low-Rds_{ON} MOSFETS, resulting in very high input stage efficiency.

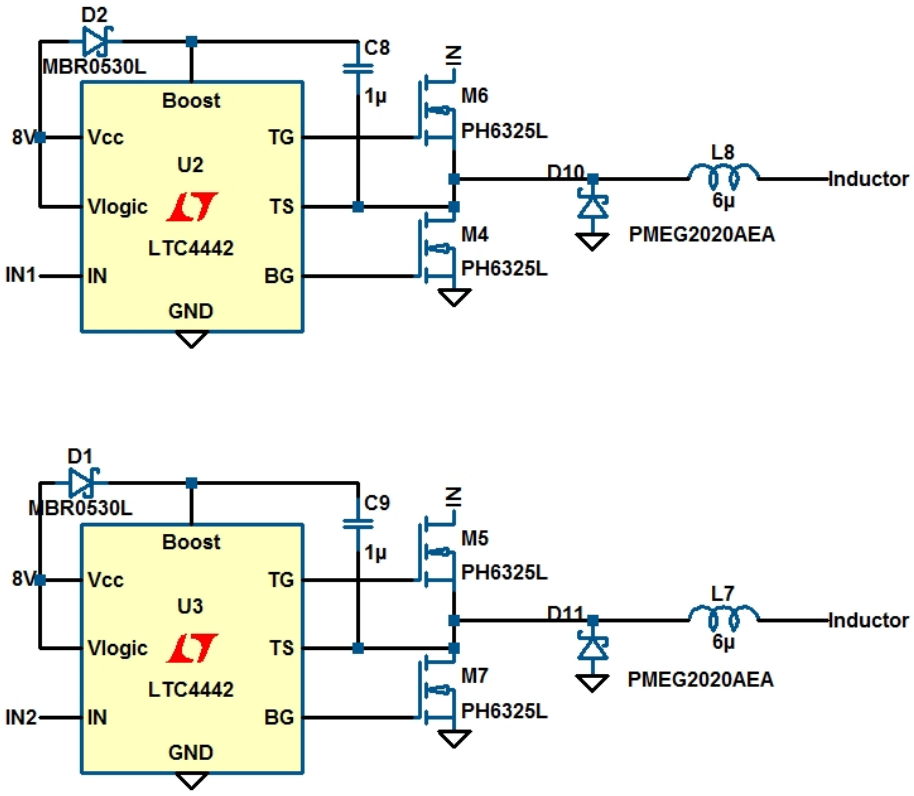

Figure 3-12: Dual Synchronous Buck Inputs

Traditionally, the Buck inductance is calculated to produce a desired current ripple. Due to the sinusoidal ripple current generated by the parallel-resonant tank circuit and the presence of the ground-referenced current-sense signal filter inductor (see Figure 3-11), the precise ripple current may only be determined through simulation and hardware testing. A value of 6 uH was deemed sufficient to produce a maximum 1 $A_{Peak\text{-}Peak}$ Buck inductor ripple current.

3.6.4. Boundary-Mode Parallel-Resonant Push-Pull Topology

The parallel resonant push-pull circuit in Figure 3-13 serves as the heart of the proposed converter. Resonant switching frequency is calculated to be:

$$f_{Res} = \frac{1}{2\pi\sqrt{L_{Res} \cdot C_{Res}}} = \frac{1}{2\pi\sqrt{(4uH)(200nF)}} = 178KHz \qquad (3\text{-}7)$$

Note that the primary inductance has been sized to the resonant inductor inductance. Assuming an unloaded switching condition, equations 3-2 and 3-3 yield an actual switching frequency of 195 KHz.

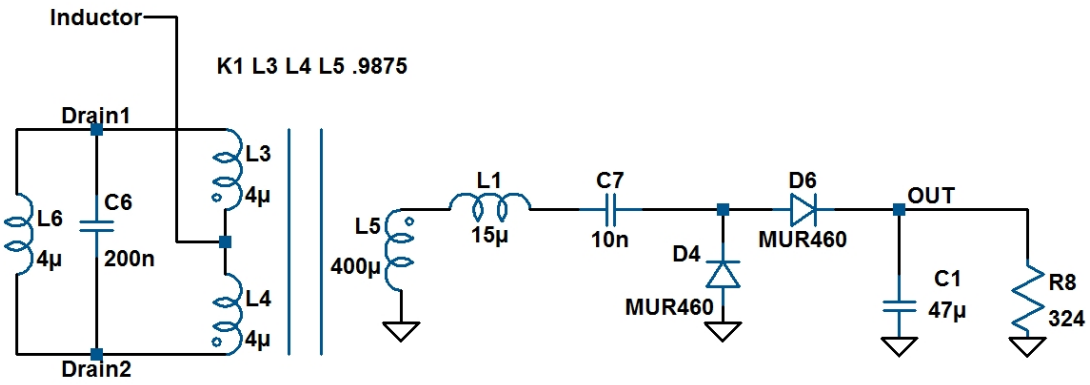

Figure 3-13: Boundary-Mode Parallel Resonant Push-Pull Topology

The resonant capacitor must handle substantial RMS currents (> 10 A) at high frequency. In order to prevent excessive I^2R power loss, metalized polypropylene film capacitors were selected. The low conductor and dielectric losses inherent to metalized polypropylene film capacitors meant that, even at full load, the resonant capacitor would barely be warmed above room temperature.

Unfortunately, the astute designer cannot afford to be quite so cavalier concerning the resonant inductor design. The high resonant currents of the boundary-mode parallel-resonant topology necessitate careful attention to the inductor's ESR. Assuming minimal proximity and skin effects, the winding power loss (W) can be found from:

$$P_{CU} = \left(I_{RMS}\right)^2 \cdot R_{DC} \tag{3-8}$$

Equation 2-11 states that the peak drain voltage will be π times the DC input. For a nominal 12 VDC input, the peak drain voltage is found to be approximately 37 V. The RMS of the half-sinewave is simply the peak voltage divided by 1.4. Therefore, the RMS inductor voltage during half a switching cycle is approximately 26 V. Assuming a resonant switching frequency of 200 KHz, the half-sinewave time interval is 2.5 µs. A Mag-Inc. PQ2020 Type-R Ferrite core served as the magnetic element for the resonant inductor [17]. For a desired core loss of 0.5 W, the core power loss can be found from

$$P_L = \frac{\text{Power(mW)}}{\text{Volume}\left(\text{mm}^3\right)} \tag{3-9}$$

The 2850 mm^3 volume of the PQ2020 core yielded a power loss of approximately 200mW/mm^3. At a 200 KHz switching frequency, the Mag-Inc. Type R Ferrite datasheet determined a 0.1 T flux density. Equation 3-10 yields 5 turns to produce 0.1 T with 26 V_{RMS}, 2.5 µs, and a core area of 62.6 mm^2.

$$N = \frac{V \cdot s}{2 \cdot A_C \cdot B \cdot 10^{-4}} \tag{3-10}$$

The resonant inductor windings were composed of 5 turns of 14 AWG Litz wire. In order to minimize high frequency losses, the Litz wire is constructed of 260 strands of 38 AWG wire. According to the manufacturer, New England Wire, the 10 cm of winding length would have approximately 5 mΩ of DC resistance [18]. A 10A RMS resonant current would result in 0.5 W of resistive loss (Equation 3-8). The combined inductor power dissipation of 0.5 W core loss and 0.5 W winding loss yields 1W of total loss at full load.

Since both the resonant inductor and push-pull transformer operate in a bipolar flux swing application, the same design methodology applies to both. A RM12 core provided ample room for the primary and secondary windings [19]. Each primary winding used two parallel strands of the 14 AWG Litz. For 2 turns per primary winding, the DC winding resistance was found to be 5 mΩ. The secondary winding contained 20 turns of trifilar (3 wires in parallel) 28 AWG wire. Total core and copper losses were roughly 1 W each, resulting in 2 W of power dissipation at full load.

3.6.5. Active Cross-Coupled Gate Drive Architecture

The boundary-mode zero-voltage switching of the parallel resonant topology is facilitated with the active gate drive circuitry shown in Figure 3-14.

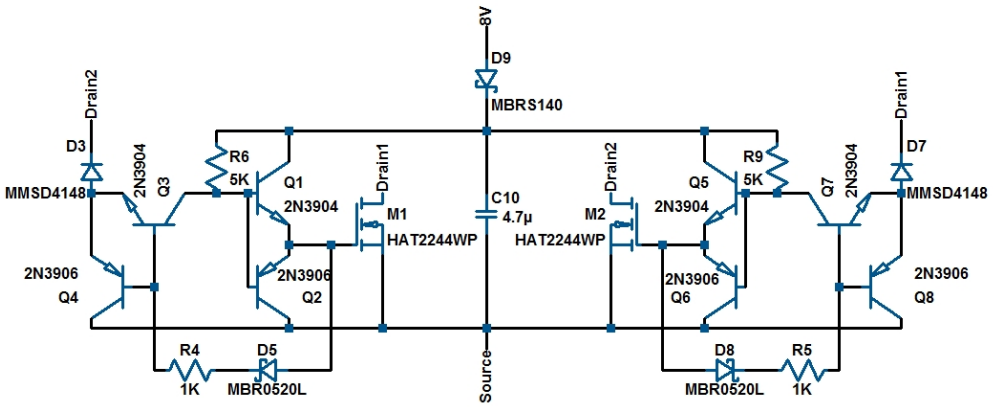

Figure 3-14: Active Gate Drive Circuitry

The ubiquitous 2n3904 and 2n3906 NPN and PNP bipolar junction transistors possess sufficient speed and power handling to sink and source the necessary Gate currents out of the power MOSFETs. Due to the analog nature of the active gate drive, the bipolar switching currents are more vulnerable to spurious noise issues than comparable digital systems. Therefore, the circuitry was implemented on a double-layered PCB with careful attention to supply bypassing and trace parasitic inductances. All diodes used in the gate drive circuitry are high-speed switching type and majority-carrier Schottky diodes.

3.7. Design Implementation

The high operating frequencies and power densities of modern DC-DC converters almost always dictate the use of multilayer PCB board construction, high density surface-mounted components, and aggressive thermal management

strategies. If the power supply designer ceases to anticipate potential sources of noise and circuit parasitics, then the likely outcome will be many frustrating hours spent trying to track down the problems. Note that the time is simply “spent”—not necessarily is it wasted. The lessons learned and skills honed by fighting elusive noise sources and phantom signal glitches have a way of becoming indelibly imprinted in one’s memory.

However, good design habits allow the designer to spend more time pursuing novel ideas and less time debugging troublesome circuits. The successful implementation of the proposed converter would not have been possible without tedious attention to the circuit layout and triple-checking of all circuit connections. The old adage proves true that “an ounce of prevention is worth a pound of cure” [20].

After finalizing the converter design, the circuit schematics dictated the PCB layout. A double-sided 2.5” by 3.8” PCB board was manufactured by ExpressPCB and arrived free of manufacturing defects. Aside from the “homemade” custom magnetics, all circuit parts were ordered from Digikey.com and Newark.com. The PCB was populated with the aid of a microscope, a hot-air gun, an adjustable temperature soldering iron, and a judicious application of No-Clean flux. After the components had been placed, all circuit nodes were tested with a multi-meter for shorts or poor solder connections. The constructed converter passed the first quality check and had been deemed ready for testing.

Chapter 4: Simulation Results

4.1. Simulated Converter Efficiency

Computer simulation allows for the designer to verify not only the desired circuit operation, but also the converter efficiency across a wide range of line and load conditions. While computer simulation results will always need to be correlated with empirical data, the speed and efficiency of computer simulation can greatly shorten design time. The simulation results of the proposed converter topology, in theory and as explained later in this section, promises to be very efficient.

The LTspice IV simulation tools proved invaluable to the design process. As the converter components were optimized to meet and exceed the initial efficiency goals, the LTspice IV software allowed for rapid verification of design changes. The proposed converter simulation results suggested an astounding 90% efficiency at full load, with greater than 85% efficiency across most of the load range. However, the simulation tools lacked the capability to simulate the push-pull transformer core loss. The transformer serves the double task of simultaneously storing resonant inductive energy and transferring power to the load. As such, the transformer must handle a significant amount of apparent power. Improper design of the transformer could result in a large amount of power loss in the magnetic core. While the hand calculations for the transformer power loss stated that the core losses would be small, the actual core power loss could potentially “make or break” the proposed converter design goals.

The simulated converter efficiency appears in Figure 4-1. Neglecting the low-load efficiency results, the overall high efficiency looked extremely promising. The 90% full load efficiency simulation results proved particularly gratifying; assuming that the actual converter would perform similar to the simulation, the converter would need only minimal attention to thermal management. The tabular simulation data for efficiency can be found in Table 4-1.

% Load	Power OUT (W)	Power IN (W)	% Efficiency
10	9.90	13.76	71.95
20	19.77	24.63	80.27
30	29.90	33.31	89.76
40	39.79	45.02	88.38
50	49.74	56.58	87.91
60	59.83	67.77	88.28
70	69.80	78.66	88.74
80	79.76	89.14	89.48
90	89.77	99.79	89.96
100	99.65	110.62	90.08

Table 4-1: Simulated Converter Efficiency Data

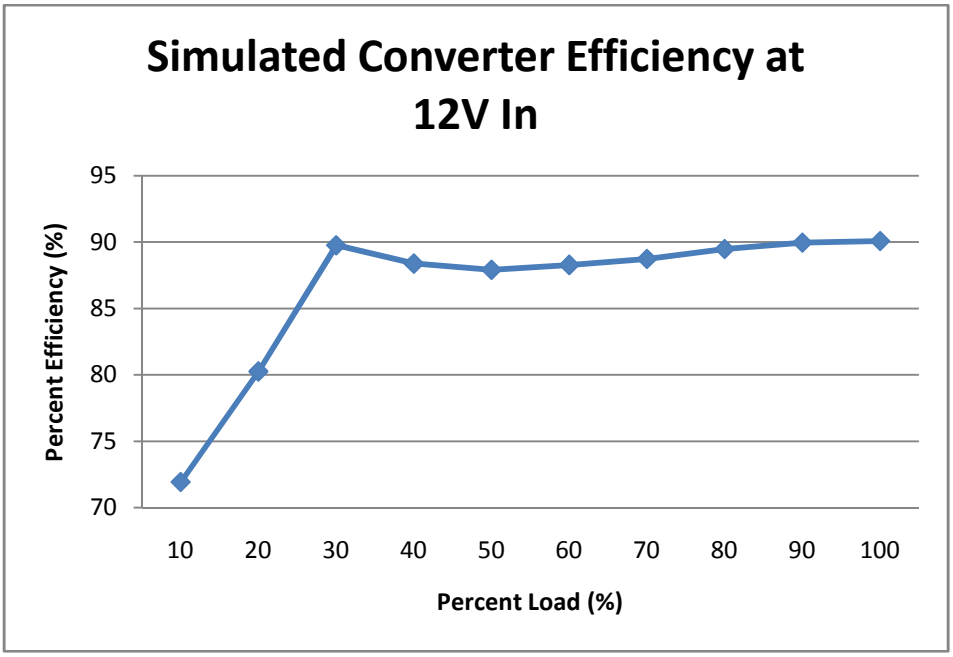

Figure 4-1: Simulated Converter Efficiency

4.2. Active Cross-Coupled Gate Drive Simulations

The novel gate drive architecture successfully switches the parallel resonant push-pull circuit at the drain-voltage boundary mode. Figure 4-2 shows the gate voltage with respect to the corresponding MOSFET drain voltage. The gate turns ON and OFF just as the MOSFET drain voltage reaches zero volts, resulting in very low switching power loss.

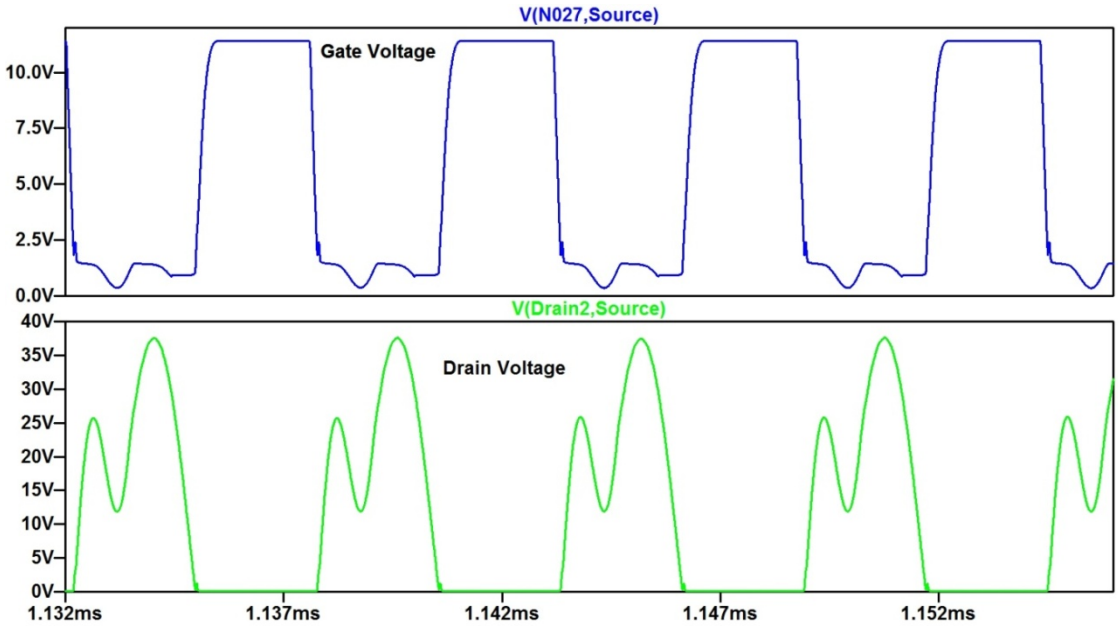

Figure 4-2: Push-Pull MOSFET Gate and Drain Voltages

The push-pull MOSFET's drain voltages and currents are displayed in Figure 4-2. The additional resonant voltage superimposed on the drain voltages is the product of the resonant voltage multiplier. This additional resonance will be harmless to the circuit operation so long as the drain voltage does not approach zero, leading to a false triggering of the active gate drive circuitry.

The slight perturbation of the MOSFET drain current in Figure 4-3 occurs as the push-pull MOSFETs do not commutate in an infinitely short switching duration.

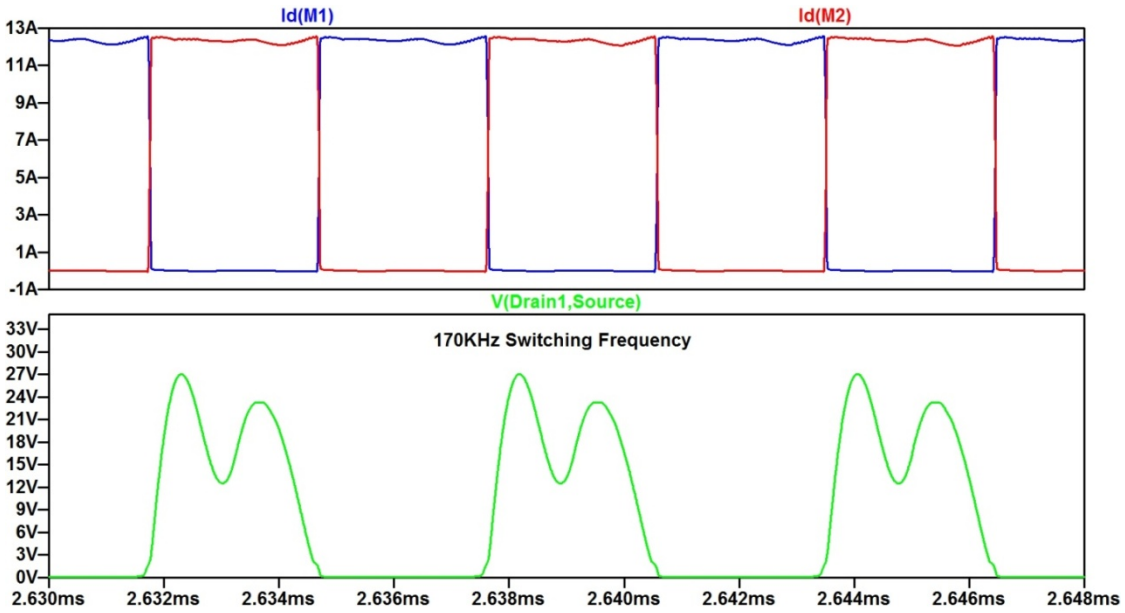

Figure 4-3: Full Load Switching Characteristics: Drain Current (Top) and Drain Voltage (Bottom)

The erratic switching behavior in Figure 4-4 underscores the need to ensure that the resonant voltage multiplier distortion does not false trigger the active gate drive. If the converter underwent this operation in real life, the push-pull MOSFETs would most certainly fail under the excessive switching losses. In order to avoid this dangerous switching condition, the voltage multiplier resonant frequency must be sufficiently offset from the boundary-mode parallel resonant frequency. This can be accomplished by changing the resonant voltage multiplier capacitor or adding external inductance to the push-pull transformer secondary.

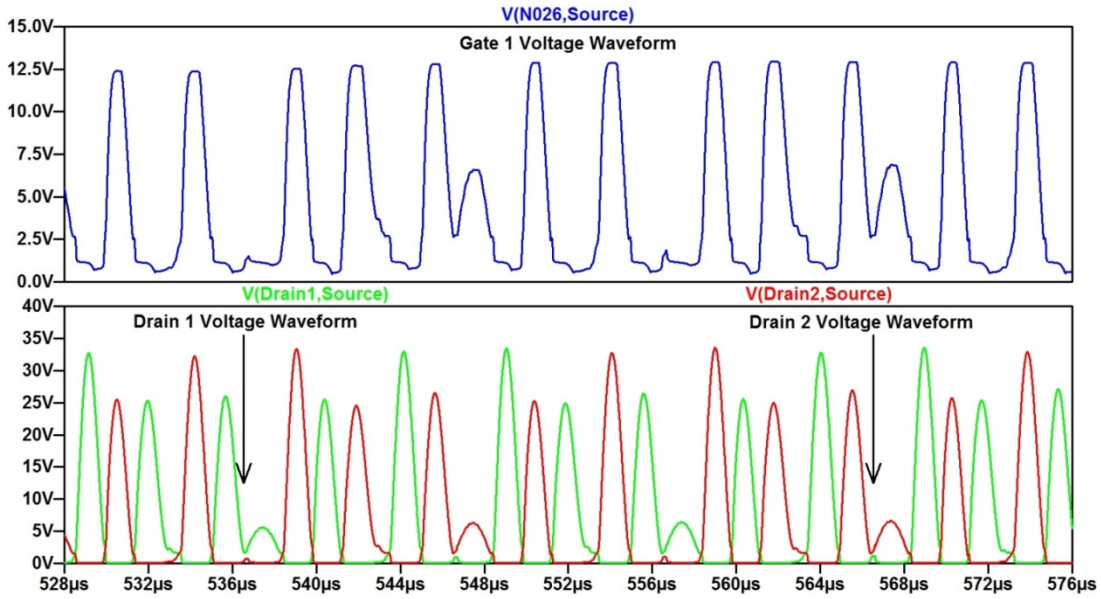

Figure 4-4: Erratic Switching Due to Resonant Voltage Multiplier

4.3. Current-Mode Control Signals

The parallel resonant tank circuit attenuates the Buck inductor current ripple as shown in Figure 4-5.

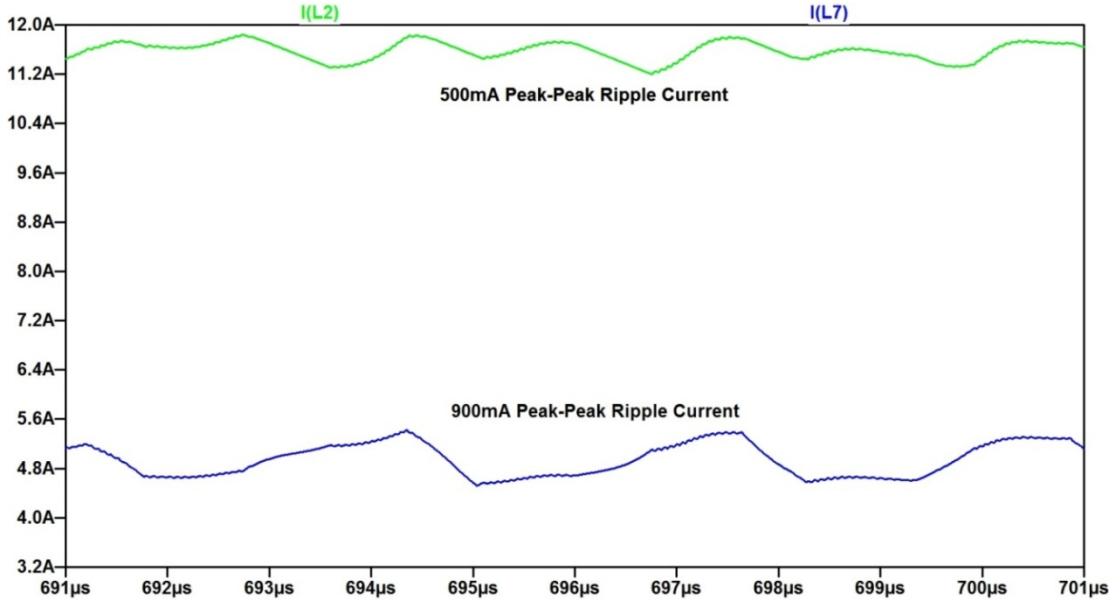

Figure 4-5: Buck and Current-Sense Inductor Current at Full Load (100W)

At full load (100 W output), a fraction of the Buck inductor current ripple does still emerge at the output of the resonant tank. Fortunately, the amount of Buck inductor current ripple is relatively small and does not negatively impact the converter's performance.

Figure 4-6 demonstrates that, at light load (30 W output), the filtering capability of the resonant circuit is much more pronounced. Since the Buck inductor output feeds into the parallel resonant tank circuit and the current-sense signal filter inductor, the Buck inductor is loaded by more of a current-source than a voltage source. As a result, the Buck inductor ripple current appears to have a significant correlation to the converter output power.

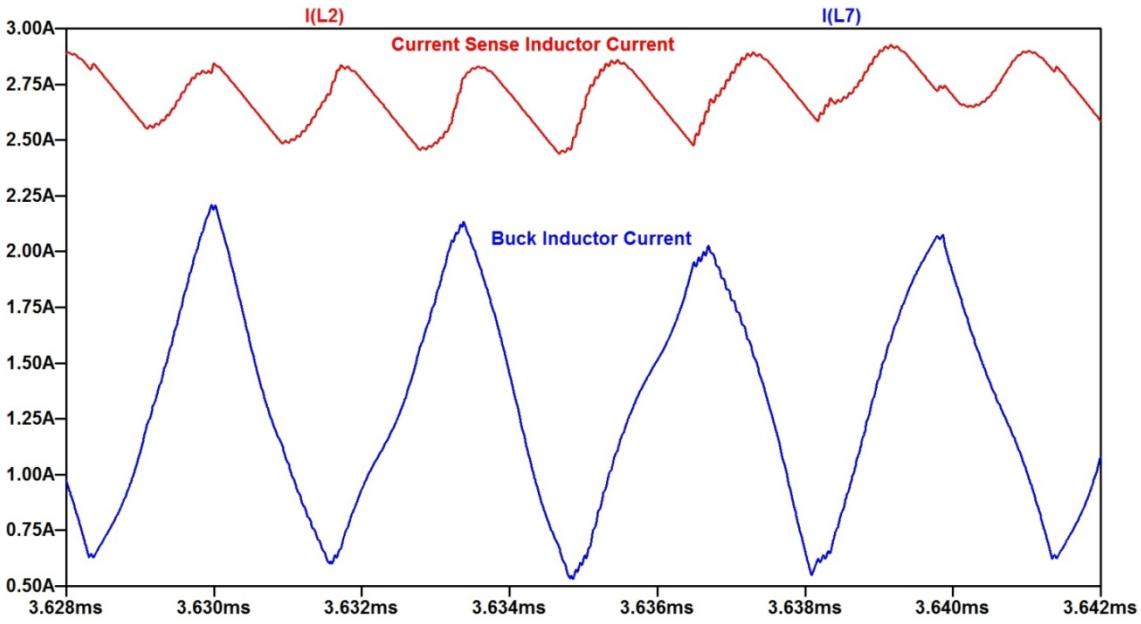

Figure 4-6: Buck and Current-Sense Inductor Current at Light Load (30W)

4.4. Known Intermodulation Problems with Current Mode Control

As Figures 4-5 and 4-6 illustrate, the current-mode control stays stable across the full load range. However, a particularly troublesome intermodulation problem can occur between the Buck topology switching frequency and the parallel resonant push-pull switching frequency (shown in Figure 4-7). The summation of the two switching frequencies leads to the generation of harmonic frequencies [21]. If these harmonics contain sizable amplitude and exist in the current-mode control loop bandwidth, the current mode controller may cause the PWM switching frequency to follow the intermodulation frequency.

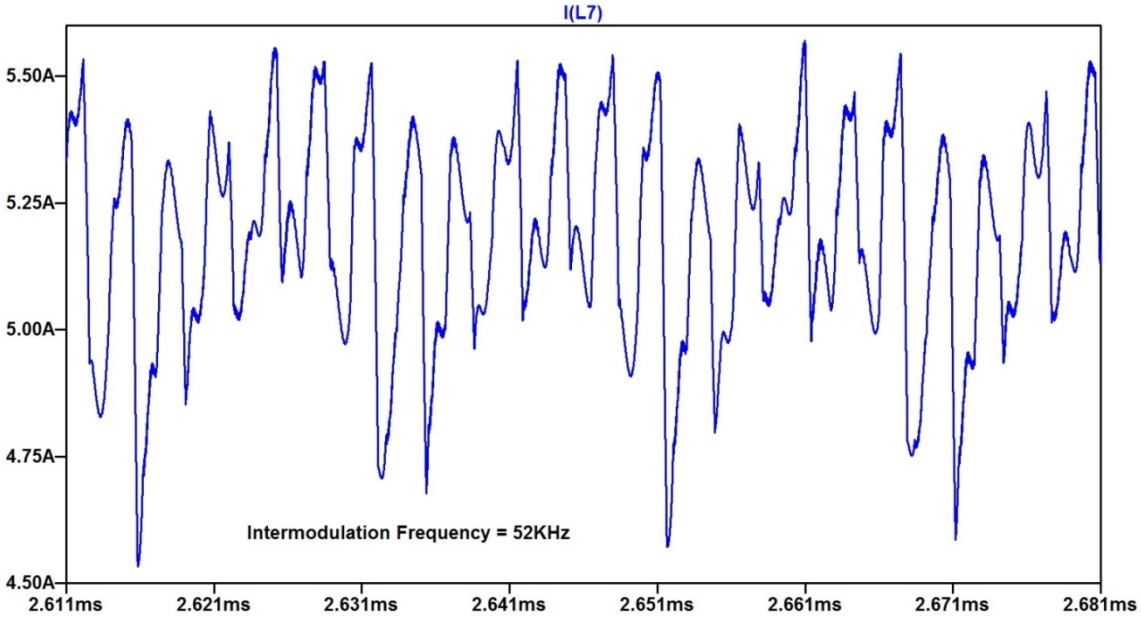

Figure 4-7: Intermodulation Frequency in the Buck Inductor Current Waveform

4.5. Converter Short-Circuit Operation

An output short circuit condition does not adversely affect the boundary-mode converter. The voltage multiplier diode current waveform in Figure 4-8 indicates that, under an output short, the converter is sourcing 850mA RMS into the low impedance short. Inherent short-circuit protection is provided by the capacitive ballast of the resonant voltage multiplier and, more significantly, the reflected load impedance shunting the majority of the magnetizing inductance. The reduction of effective primary magnetizing inductance results in a reduced applied primary winding voltage (as most of the voltage is applied to the transformer leakage inductance). Since the push-pull transformer possesses a 1:1:10 turns ratio, the primary windings must logically be conducting 8.5A RMS. This current only circulates in the low-loss resonant tank circuit; as such, the simulated quiescent power drawn by the converter is shown in Figure 4-9 to be approximately 7W. The majority of this power is dissipated in the resonant components, namely the resonant inductor and the push-pull transformer. Fortunately, the resonant inductor and transformer possess more than sufficient area to remain cool while dissipating the quiescent short-circuit power loss.

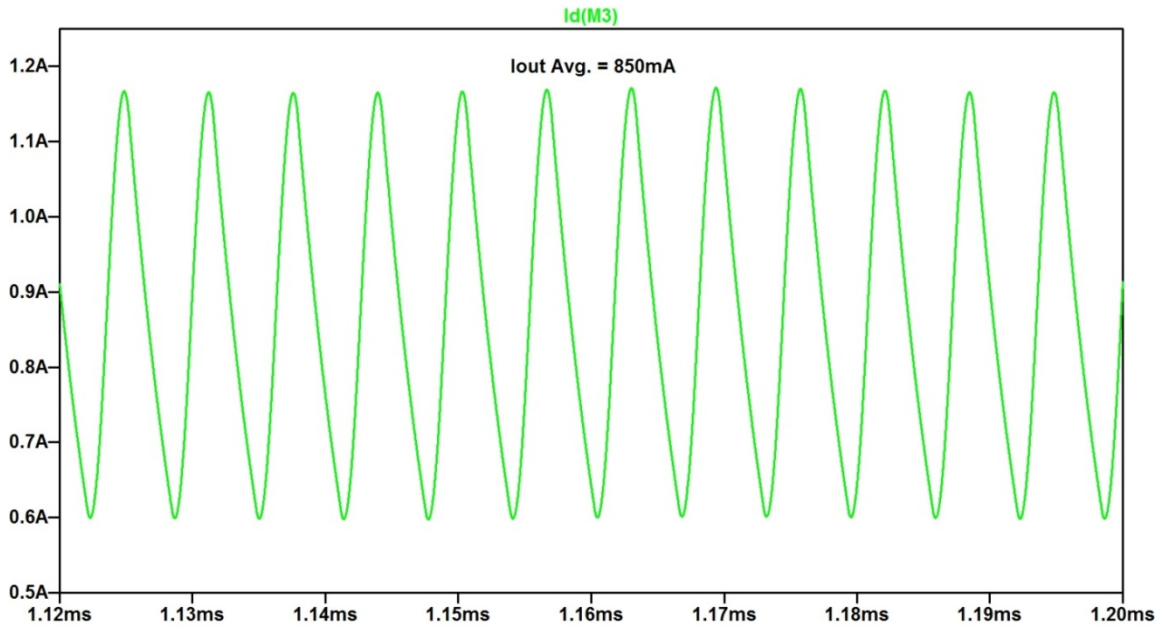

Figure 4-8: Steady-State Output Short-Circuit Current

Intuitively, the output short-circuit should shunt a portion of the push-pull transformer's magnetizing inductance. The resultant decrease in the primary tank circuit inductance would slightly raise the converter resonant frequency. However, the secondary-side resonant multiplier acts in series with the output short to actually lower the boundary-mode resonant frequency of 164 KHz (shown in Figure 4-9) compared to the full load boundary-mode resonant frequency of 170 KHz (Figure 4-3).

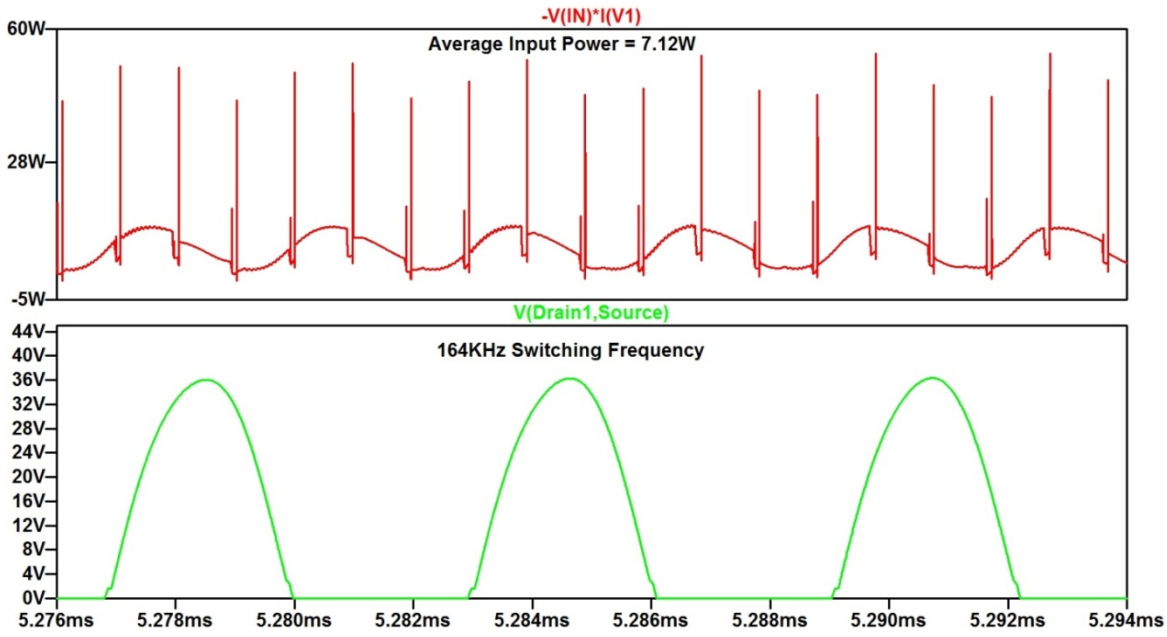

Figure 4-9: Short Circuit Input Power and Switching Frequency

The LTspice IV simulation results indicate that the converter will not only meet expectations, but actually exceed them, provided that the simulation faithfully represents the conditions and circuit operation encountered in real life. The hardware testing will ultimately determine whether the proposed converter will operate as desired.

Chapter 5: Hardware Results

5.1. Converter Test Setup and Equipment

Before the converter could be tested, an active load needed to be located. Active loads capable of dissipating over a hundred watts at 180 VDC are quite rare; as such, an active load was improvised from a high-voltage, high power IGBT (GA75TS60U) and an adjustable voltage source (Figure 5-1).

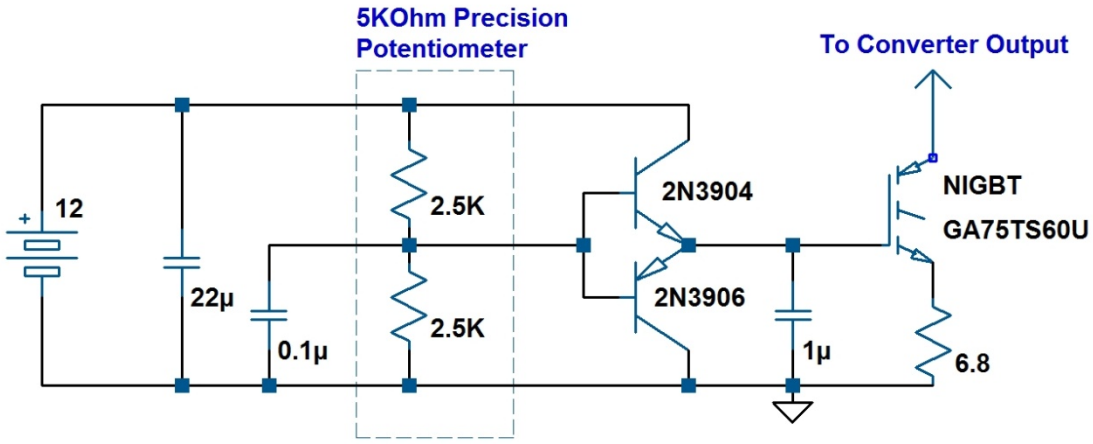

Figure 5-1: IGBT-Based Active Load

The GA75TS60U Punch-Through IGBT datasheet quotes an -11 mv/℃ threshold temperature coefficient [22]. A negative threshold temperature coefficient will, for a fixed gate-emitter bias voltage, lead to increasing collector current as the device junction heats up. Consequently, a 6.8 Ω resistor was inserted between the IGBT emitter and ground. Any increase in collector current due to the negative threshold temperature coefficient would create in increased voltage drop across the 6.8 Ω resistor, lowering the effective gate-emitter bias

voltage. Additionally, the IGBT device was mounted on a copper heat sink with forced air cooling. The active load sink current could be controlled by adjusting the precision multi-turn 5 KΩ midpoint voltage, setting the gate-emitter bias voltage of the saturated IGBT.

A HP 6574A DC power supply served as the converter input power source. The DC power supply could source up to 35 A at 60 V DC, more than sufficient for the converter power requirements. A Fluke 87 multi-meter confirmed that the HP 6574A power supply display showed the correct voltages and currents across the full line range. Additional Fluke 87 multi-meters simultaneously measured the converter output voltage and current, as well as the input voltage using a board-level Kelvin connection. Circuit waveforms were obtained using a calibrated Instek GDS-2204 200MHz 4-Channel digital storage oscilloscope. High-bandwidth board-level oscilloscope probe jacks replaced the typical probe ground leads, as the ground lead inductance could introduce a frequency-dependent ground offset between the oscilloscope probe and the converter ground plane. Figure 5-2 shows the converter test setup with identifiable circuit components highlighted for perspective.

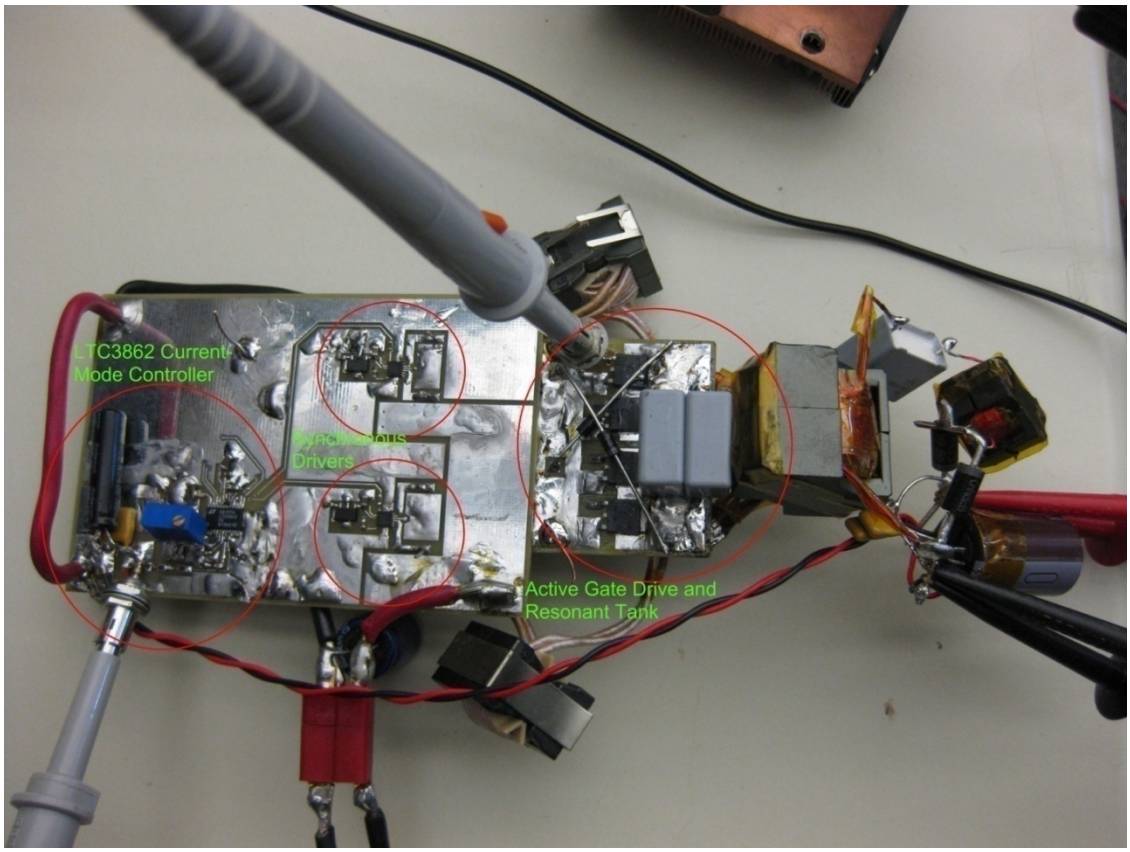

Figure 5-2: Converter Test Setup

5.2. Converter Efficiency

The converter, upon start-up, immediately output a stable 179.9VDC at 12.2VDC in. Adjustment of the active load yielded 0.25 A out at 179.9 VDC—100 W of output power. Input power calculations revealed that the converter drew 112.6 W of input power; this yielded 89.1% converter efficiency at full load. Immediately, it was clear that the converter had exceeded the desired 85% converter full load efficiency. Further efficiency measurements (shown in Table 5-1 and Figure 5-3) revealed that the converter operated at 90.1% efficiency at 80% load, with a minimum converter efficiency of 81.3% at 10% load.

% Load	Vin (V)	Iin (A)	Vout (V)	Iout (mA)	P_OUT (W)	P_IN (W)	% Efficiency
10	12.000	1.115	179.9	60.5	10.88	13.38	81.3
16	12.010	1.608	179.9	90.5	16.28	19.31	84.3
20	12.000	2.196	179.9	125	22.49	26.35	85.3
30	12.000	3.138	179.9	179	32.20	37.66	85.5
40	11.995	4.239	179.9	242	43.54	50.85	85.6
50	12.011	4.999	179.9	290	52.17	60.04	86.9
60	12.000	6.020	179.9	353	63.50	72.24	87.9
70	12.000	7.050	179.9	422	75.92	84.60	89.7
80	11.990	7.590	179.9	456	82.03	91.00	90.1
90	11.990	8.600	179.9	514	92.47	103.11	89.7
100	12.226	9.215	179.9	558	100.38	112.66	89.1

Table 5-1: Converter Efficiency Measurements

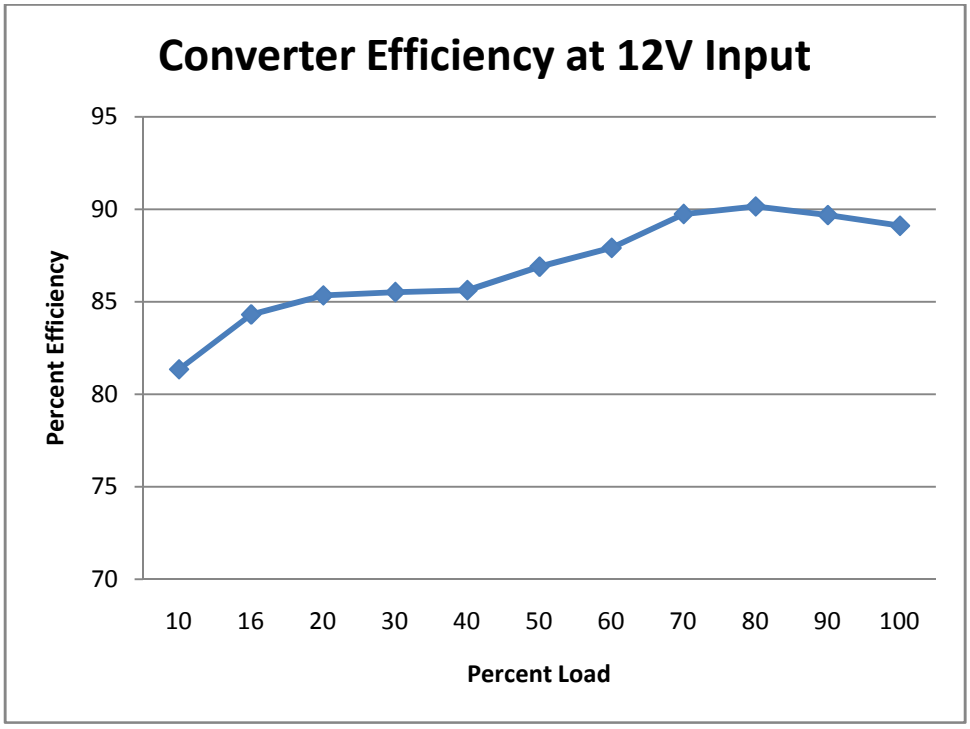

Figure 5-3: Plot of Converter Efficiency with Respect to % Load

The simulated and measured converter efficiencies are shown in Figure 5-4.

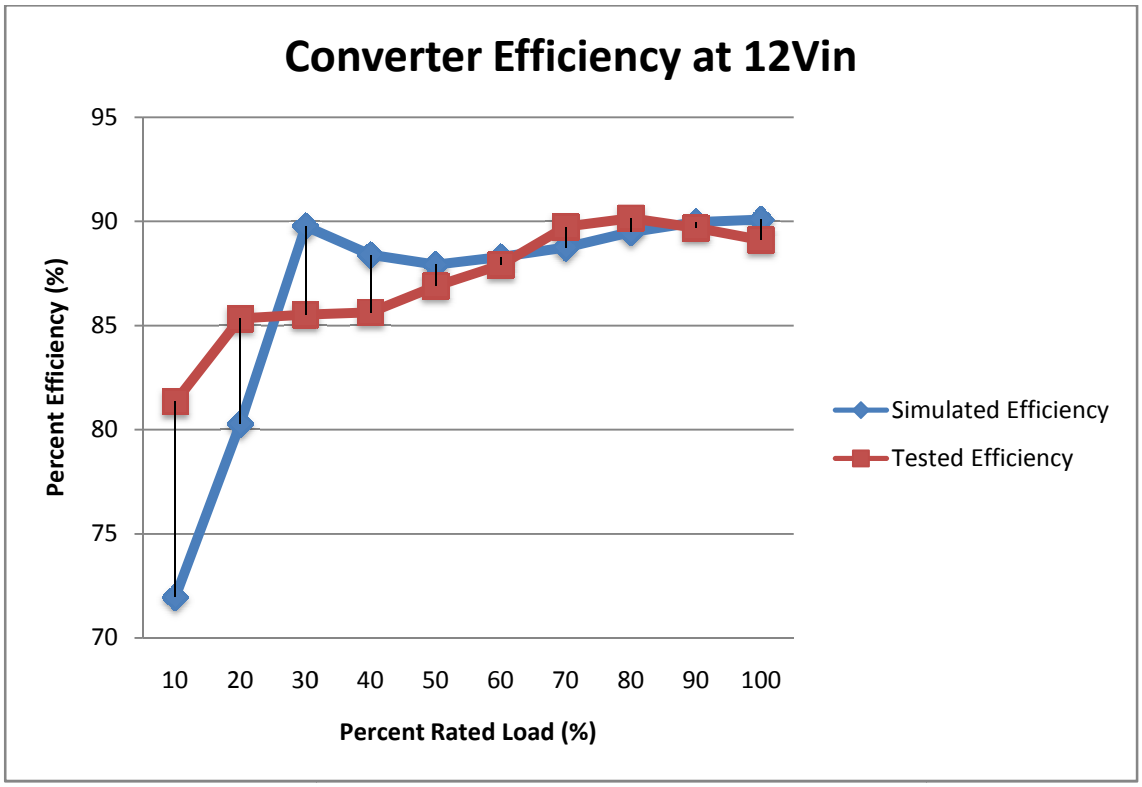

Figure 5-4: Converter Efficiency, Simulation vs. Hardware

5.3. Boundary Mode Resonant Push-Pull Waveforms

The MOSFET drain voltage in Figure 5-5 shows that the resonant tank circuit oscillates at 167 KHz, very close to the simulated switching frequency of 170 KHz in Figure 4-3. Additional superimposed drain voltage resonance, due to the resonant voltage multiplier, causes the drain voltage to drop to 16 V. Since the active gate circuitry will not trigger a switching transition until the drain voltage reaches near-zero volts, the resonant voltage multiplier operation will not interfere with the primary side resonance. In fact, the secondary side resonant components may be sized closer to the primary resonant frequency, leading to increased secondary resonant peaking and a higher overall power throughput.

The disadvantage will be increased voltage stress on the secondary resonant components and output diodes.

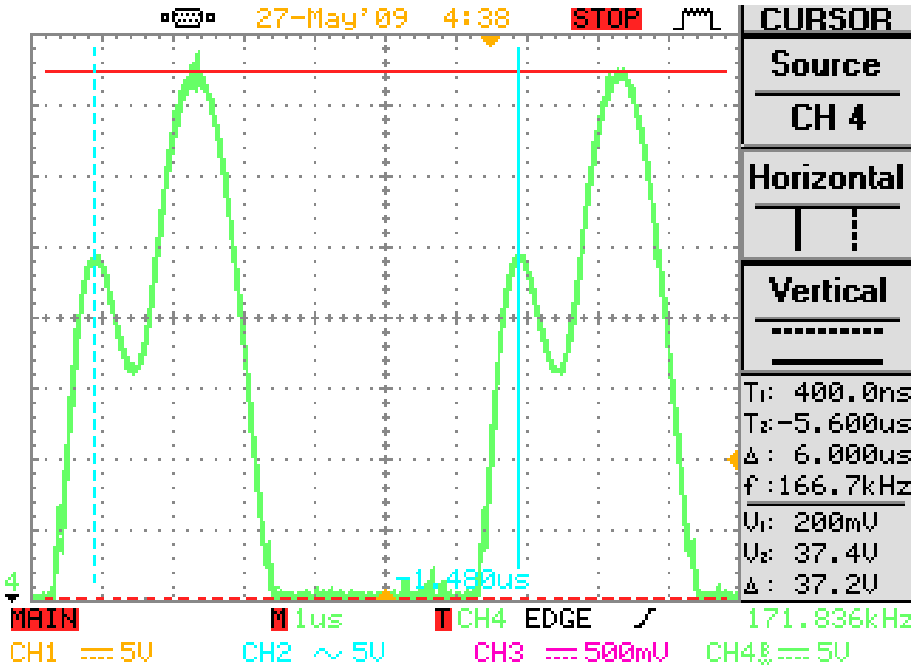

Figure 5-5: Drain Resonant Voltage Waveform

The MOSFET gate voltage in Figure 5-6 indicates that the active gate drive circuitry performs admirably. Zero-voltage switching occurs at the boundary mode of the parallel tank resonance. Note that the gate and drain waveforms pertain to the opposing MOSFETs.

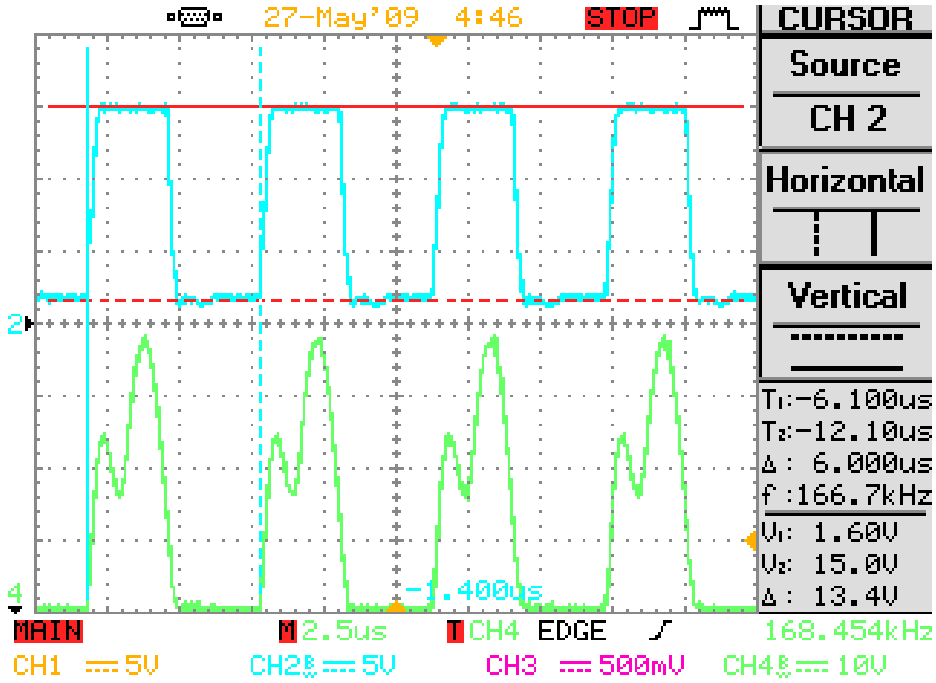

Figure 5-6: MOSFET Gate (Top) and Drain (Bottom) Voltage Waveforms

The 428 mV output voltage ripple in Figure 5-7 constitutes only 0.2% of the 179.9 VDC output. Since the secondary side resonant voltage multiplier generates a roughly sinusoidal output, the output switching noise contains far less wideband harmonic content than the typical PWM converter counterpart. The reduced wideband frequency content of the converter output simplifies the filtering requirements for loads sensitive to high-frequency noise.

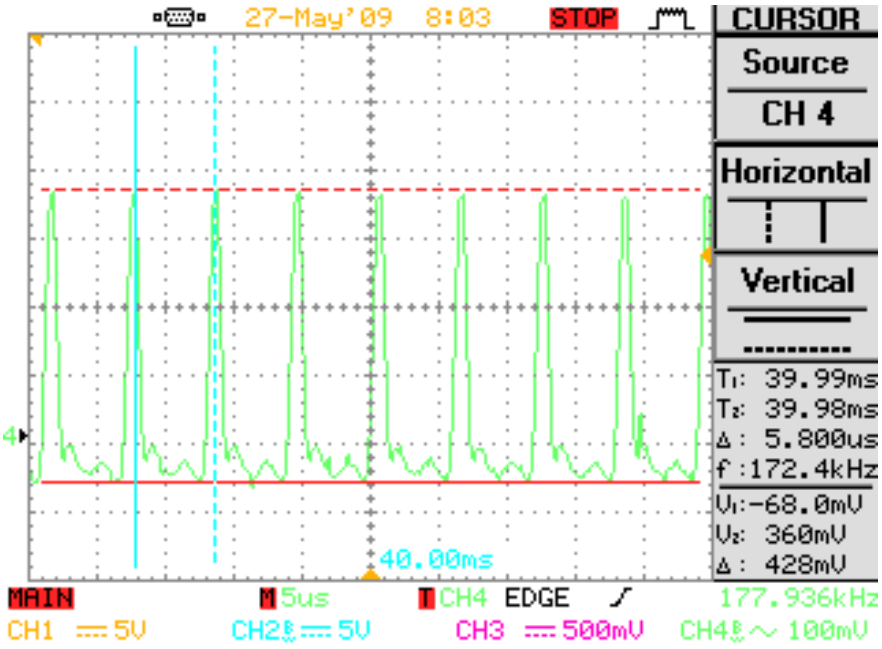

Figure 5-7: AC-Coupled Resonant Switching Output Ripple

5.4. Output Short-Circuit Condition

The converter response to an output short-circuit is shown in Figure 5-8. A 20 ms duration short-circuit condition causes the output voltage to plummet from 180 VDC down to zero volts. After the short-circuit condition has elapsed, the converter output begins a controlled rise back to the regulated output voltage. The oscilloscope waveform indicates that the output overshoots the target regulated voltage by 6 V—only 3% over the nominal 180 V output. Hardware testing revealed that the converter sources a steady-state current of 715 mA into an output short. The quiescent short-circuit power draw consumes 0.61 A from the 12 VDC source (7.32 W).

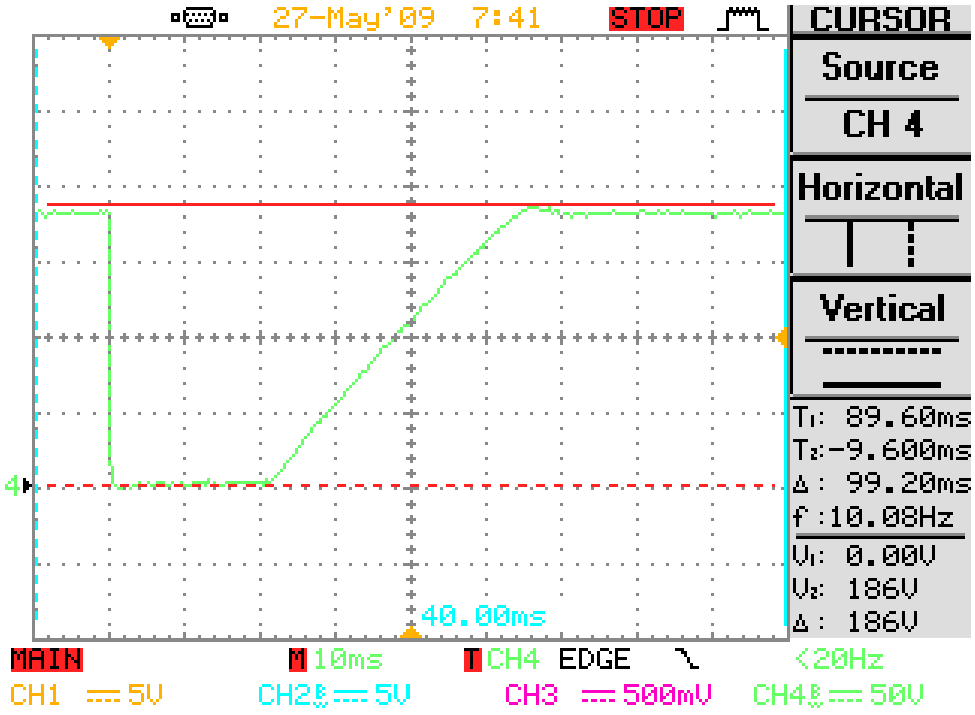

Figure 5-8: Output Voltage with a 20ms Output Short Circuit

The resonant frequency switching drops from the full-load switching frequency of 167 KHz in Figure 5-5 to the short-circuit switching frequency of 154 KHz in Figure 5-9. Note the absence of the secondary-side voltage multiplier resonance on the drain voltage.

Equation 2-11 states that the peak drain voltage will be equal to π times the input voltage. For a 12.2 VDC input, the peak drain voltage is calculated to be 38.3 V. This value correlates well with the 38.4 V peak shown in the oscilloscope waveform.

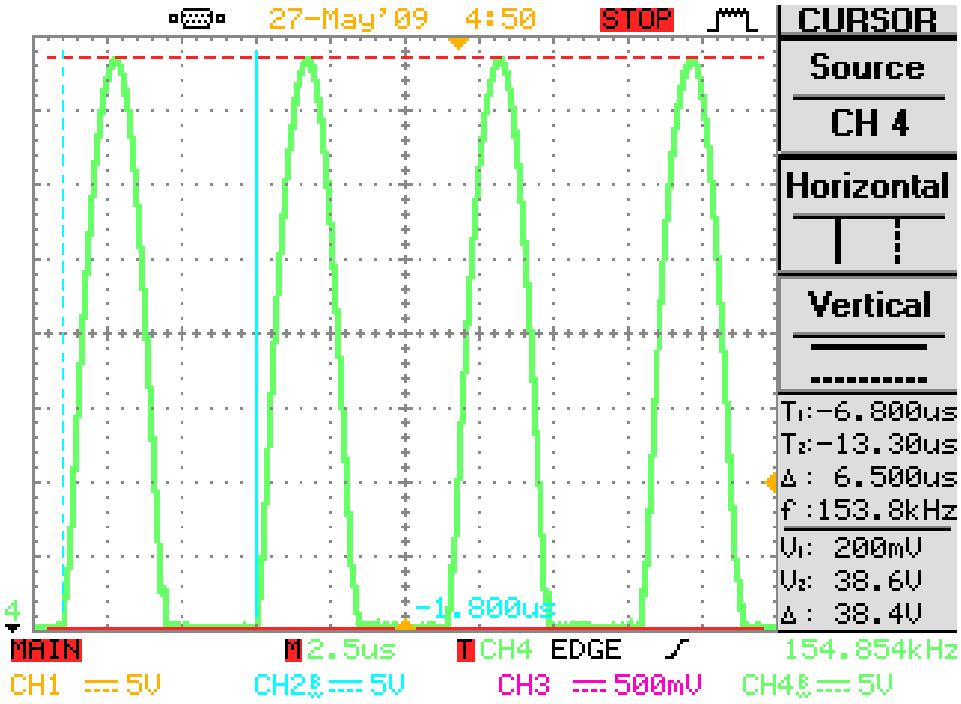

Figure 5-9: MOSFET Resonant Drain Voltage during Output Short-Circuit

5.5. Intermodulation Problems Inherent to Current-Mode Control

The intermodulation produced by the summation of the Buck input and Resonant Push-Pull switching frequencies could be witnessed during hardware testing. During stable current mode control, the Buck inductor current resembled the current waveform in Figure 5-10. The current-mode controller switching frequency was manually adjusted via a potentiometer until a Buck switching frequency yielded distinct intermodulation instability (shown in Figure 5-11). Interestingly, the converter continued to regulate the feedback; however, the irregular Buck input switching decreased the converter efficiency.

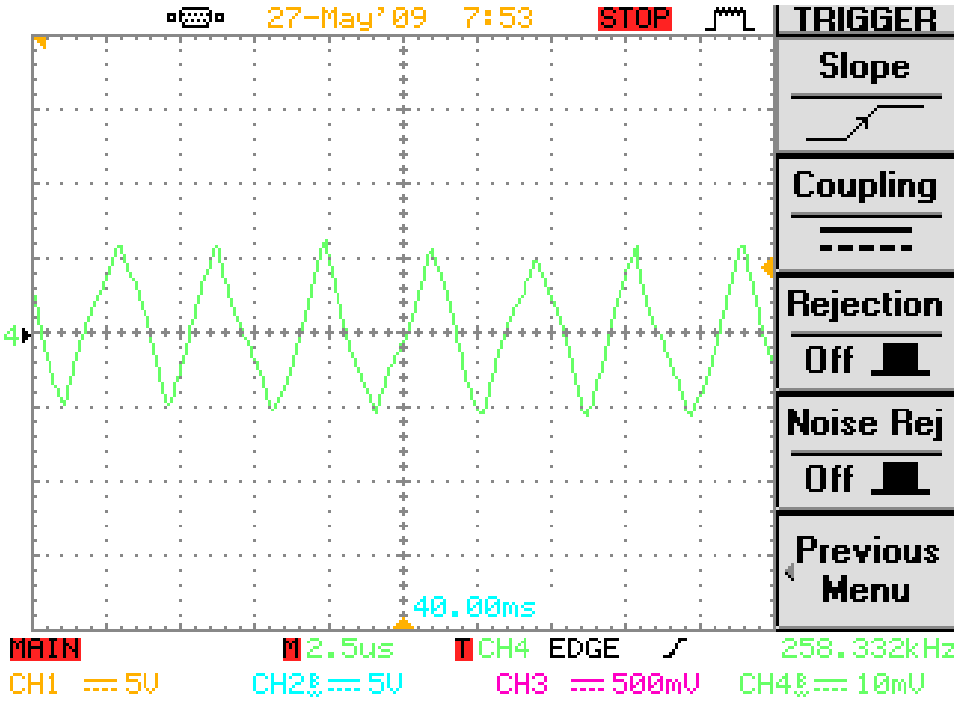

Figure 5-10: Buck Inductor Current 1; 1 Amp/Vertical Division

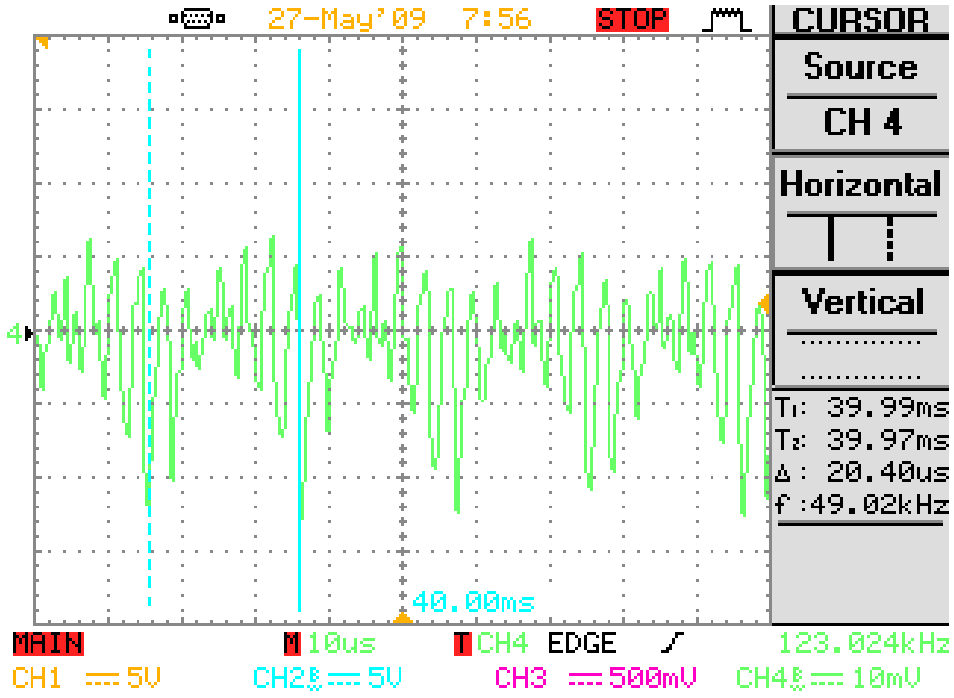

Figure 5-11: Buck Inductor Current 2; 1 Amp/Vertical Division

Chapter 6: Summary

The pervasiveness of power electronics signifies that every improvement on performance will have a widespread impact on total power usage and quality. As such, even small advancements in efficiency and performance are worth striving for. The original converter project goals were neither lofty nor unobtainable: 85-90% step-up converter efficiency, indefinite short-circuit protection, and flexible switching operation. With the aid of computer simulation tools and copious circuit analysis, the vague theoretical converter framework evolved into a fully-functional hardware prototype. The proposed converter topology not only met, but exceeded, the original project goals.

Inspiration for the proposed converter topology came from a variety of sources: textbooks, internet research, electronic component datasheets, etc. The distillation of the converter topology from a myriad of possible ideas, however, took a considerable amount of trial and error. Many converter building block variations were sketched on scratch paper, thoughtfully considered, and promptly crumpled up, only to be pitched unceremoniously into the recycle bin. Fortunately, persistence (or at least the law of averages!) yields good ideas eventually. The first cohesive model of the proposed converter closely resembles the block diagram shown in Figure 3-1.

The successful integration of the theoretical building blocks, however, could only have been made possible by countless hours spent running computer simulations and lab testing candidate circuit configurations. The converter

simulations showed promising results; as such, the circuit was built and successfully tested. Hardware results correlated surprisingly well with simulation data.

Occasional setbacks, particularly the intermodulation problems first detected in simulation, served to prompt ideas for future development more than anything else. The resonant tank circuit successfully attenuated the majority of the Buck inductor current signal; however, the relative proximity of the Buck input and push-pull resonant switching frequencies ensures that the potential for intermodulation instability will always exist. This threat could be eliminated entirely by switching to strictly voltage-mode control.

Due to the flux-imbalance problem inherent to the push-pull topology, voltage-mode control is seldom used in push-pull converters. Current-mode control provides another benefit as well; peak-current detection protects the push-pull MOSFETs from destructive switch currents during an output short-circuit condition. The proposed converter topology, however, requires neither short-circuit nor flux-imbalance protection. The boundary-mode parallel resonant tank circuitry ensures that the applied transformer volt-seconds balance from switching cycle to cycle. Additionally, the primary resonant circuitry, as well as the resonant voltage multiplier, protected the converter from an output short.

The high-bandwidth current-mode control loop facilitates fast transient response and simplifies control loop compensation. However, many high voltage applications require slower output transitions upon start-up and after output fault conditions. Furthermore, a high switching frequency could still yield a fast

voltage-mode control loop. The ground-referenced current sense resistor and corresponding filter inductor could be eliminated by implementing voltage-mode control. These simplifications, as well as the elimination of possible intermodulation problems, promote the use of voltage-mode control in the proposed converter topology.

The proposed converter topology successfully met the original project goals. Therein lies the question: what is the next step? As long as there is potential to improve the proposed converter topology and pursue new ideas, the process of innovation never truly ceases.

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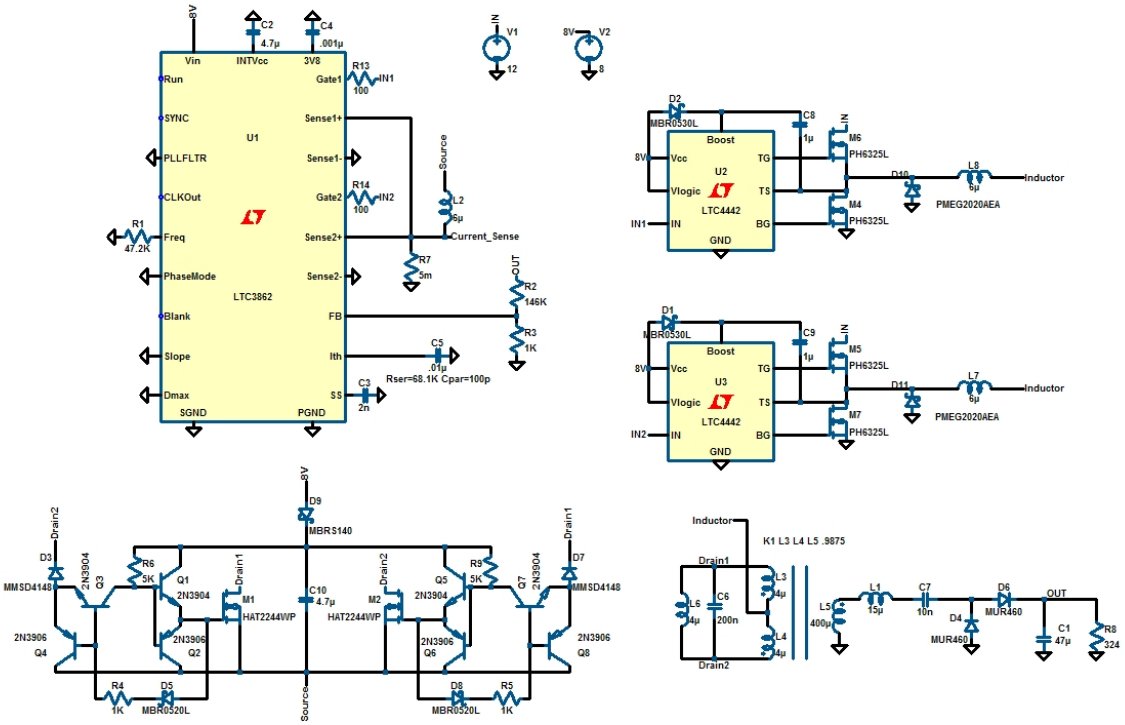
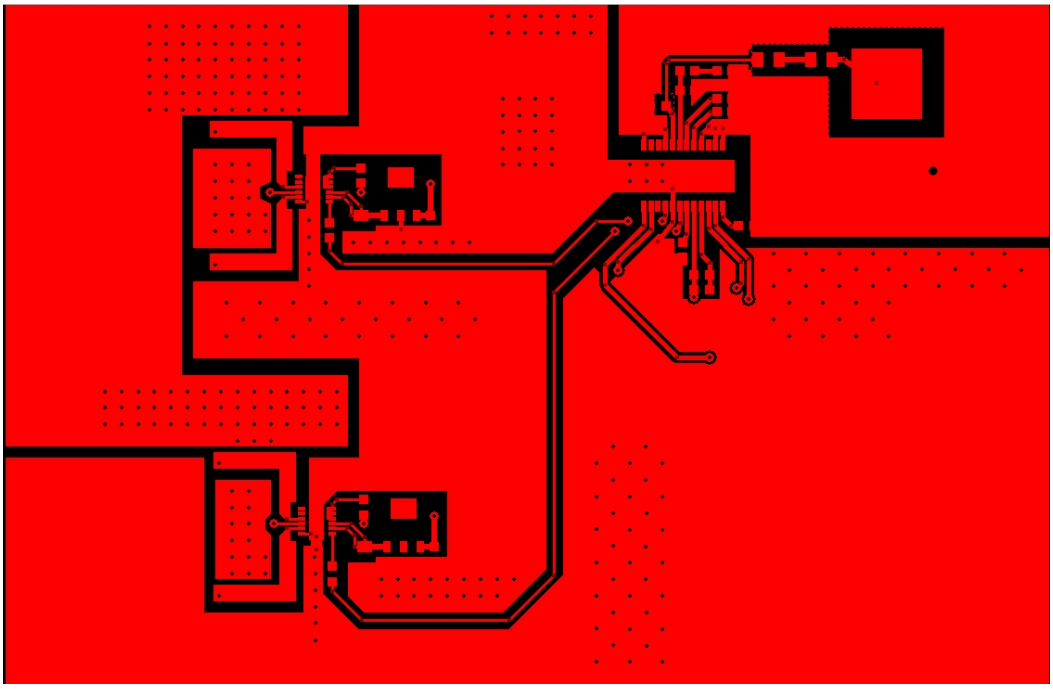
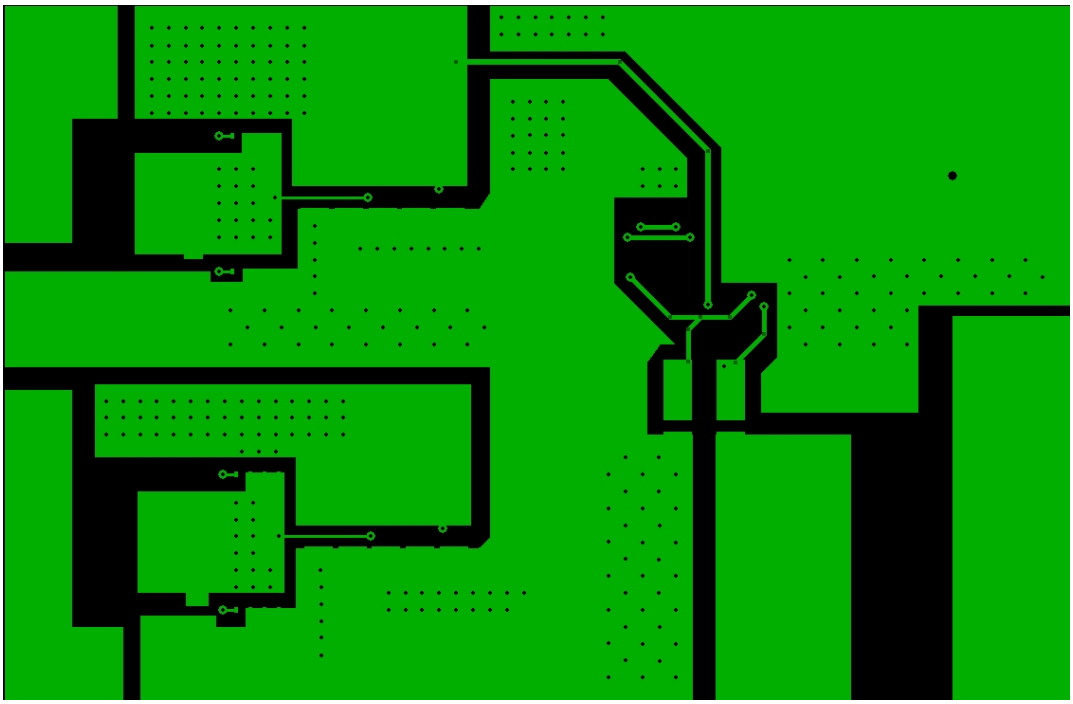
Appendix A

8.1. Converter Schematic



Appendix B: Converter PCB Top and Bottom Layers





Appendix C: Resonant Push-Pull PCB Top and Bottom Layers